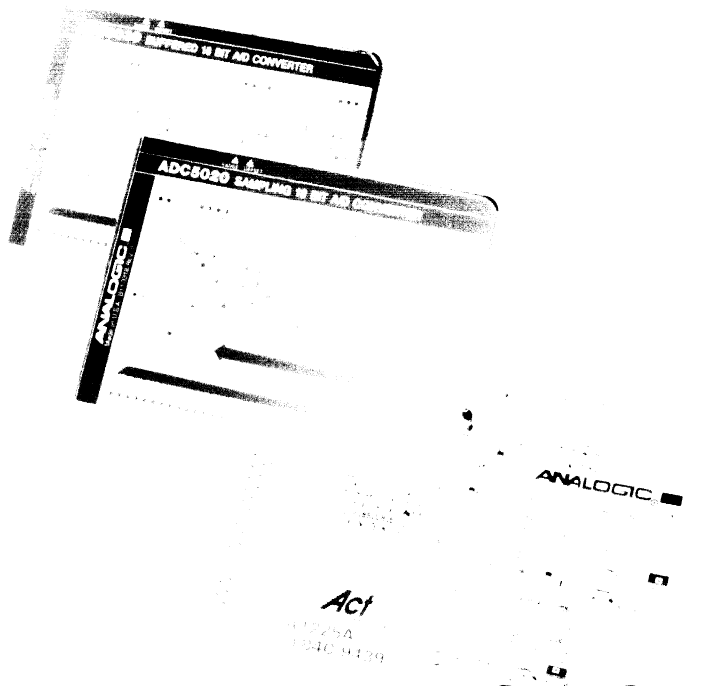


Data Conversion Components Catalog

DATA CONVERSION PRODUCTS GROUP
ISO 9001
CERTIFIED

ANALOGIC

The World Resource
for Precision Signal Technology

About Analogic...

Analogic is an innovative company with core competencies in high speed, high precision signal acquisition, conditioning and measurement. Since its inception over 25 years ago, the Company has earned a reputation as a prime source of state-of-the-art, application-oriented signal devices with superior accuracy and stability. Collectively, the Analogic staff has been responsible for hundreds of landmark patents and many times that number of exclusive circuits and devices.

Our capabilities in precision, high speed numeric measurement of wide-dynamic range analog signals; accurate, high speed conversion of both analog and digital signals; and advanced signal processing are at the core of most of the Company's new product activities. Our unique experience in these fields can constitute a distinct competitive advantage for our customers.

At Analogic we know the challenges of real-world applications — for more than 25 years, we have been partnering with leading OEMs, developing and manufacturing advanced cost-effective solutions. On more than one occasion, our innovative designs have helped revolutionize our customers' businesses — and even entire industries.

Analogic, with annual revenues over $200 million, comprises over 1400 people — including more than 300 engineers and scientists — committed to innovatively exploiting state-of-the-art technology for our customers. Our team includes about 1000 people at our central design and manufacturing facilities and corporate headquarters in Peabody and Wakefield, Massachusetts, and about 400 people at the design and manufacturing facilities of our subsidiaries: SKY Computers, in Chelmsford, Massachusetts; Camtronics, Ltd., in Hartland, Wisconsin; and B&K Medical AS, in Gentofte, Denmark. We also have a joint venture affiliate in China.

Profile of an A/D/A Supplier

Breadth of Experience

The innovative expertise at Analogic spans almost three decades of pioneering experience in the field of data conversion. As a result, today Analogic has, in volume production, an extremely wide range of standard products that can help many customers solve instrument and systems problems with the optimum combination of performance, reliability, and economy.

A History of Creative Engineering

Some of our basic data acquisition patents are listed on page iv. They are but a few of the multitude of patents awarded to Analogic's engineers, many of whom have played — and are playing — a pivotal role in the development of data acquisition technology.

An Understanding of Instrumentation

Precision signal translation instrumentation is more than a mere collection of modules or equipment. It involves an understanding of the source characteristics, the "fidelity criteria" of the particular requirement, and a practical understanding of information theory, noise effects, ground loops, interference, and signal processes, as well as other theoretical and practical aspects. Our experience has shown that high precision devices with genuine integral accuracy are hard to design and even harder to manufacture. That's why we want our customers to know about the potential pitfalls when designing-in our products and why we offer full assistance to arrive at the "best (cost/performance) solution" to signal translation and digitizing instrumentation problems.

Engineering Judgment

Today, the engineer is faced with a bewildering array of signal conditioning devices, multiplexers, filters, amplifiers, A/D and D/A converters, and digital processors. Some devices employ the latest state-of-the-art techniques while others that do not still may offer an economic or technical advantage. Some are unique and have no second source or do not have proper interface capability. However, Analogic offers a practical alternative to the confusion of choices. For those who have a special need, where no "right" solution is readily available, Analogic offers the creative ability and engineering judgment to arrive at the simplest, yet most sophisticated practical answer.

Automated Precision Test Capability

Signal translation equipment requires detailed testing to meet specifications on each and every quantization level over a wide range of power supply and temperature variations. To carry out these tests economically and to assure customers of the integrity of the products they buy, Analogic has invested heavily in advanced automated precision test equipment. The analog characteristics, absolute accuracy, precision and linearity of our many diverse products are thoroughly tested with literally millions of measurements — all traceable to the National Institute of Standards Technology (NIST), and customers are provided with test data documentation to assure reliability.

Emphasis on Reliability

Analogic engineering has always stressed "worst case" designs and "error budgets." In fact, our founders coined those phrases years ago and have written extensively on their implications. Reliability in precision instrumentation means more than functional life. It relates also to the equipment, modules, subsystems or systems meeting their specifications reliably over extended periods of time — in widely different environments and sources of powering. Analogic engineers welcome the opportunity to demonstrate worst case and error budget design realities to our customers.

Unmatched Facilities

Visitors to Analogic are often surprised at the scope and diversity of our facilities — well-cared-for voltage standards traceable to NIST, extensive burn-in facilities for the total product line, environmental equipment and, particularly, automatic computer-controlled test equipment with comprehensive software programs covering modules, subsystems and systems.

Ability to Provide Custom Specialized Designs

In addition to developing advanced devices for its broad standard product line, Analogic's engineering capability is also geared to custom designing exclusive devices or systems for specific customers. Such private brand designs are usually developed by our management, engineering, marketing, and production staffs in close cooperation with our customers. Our experience has shown that quite frequently we can offer the complete unit at a better performance/cost value than is practical for the customer to undertake independently.

Customer Service and Technical Support

Customer support at Analogic means much more than supplying delivery information. It means logistical support, quick turnaround on repairs (typical repair cycle is 3-4 days), training of customer engineering personnel, interfacing with customer incoming-inspection personnel, coordination of test requirements, quick modifications for special requirements and a host of other services that can only be realized by doing business with Analogic.

Technical Skills and Expertise

Engineering and technical development at Analogic occur within a matrix of mutually supporting technologies. Analogic's technical staff, including over 300 engineers and scientists, has mastered the elements required to address needs in areas such as:

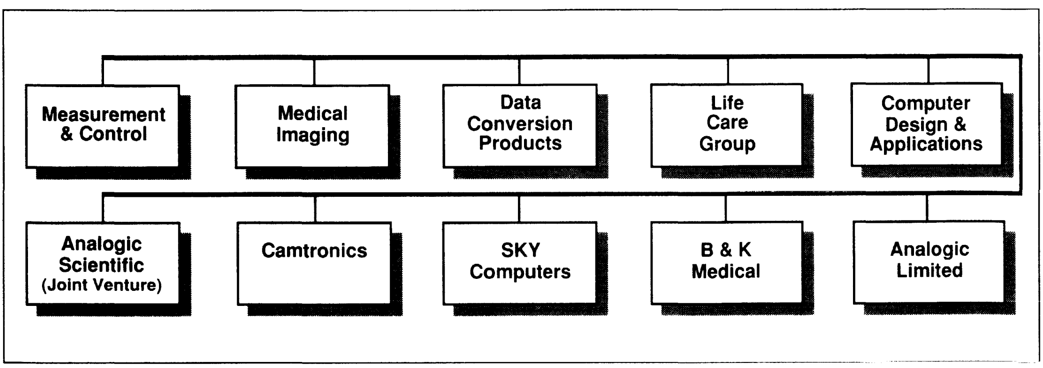
- High performance medical imaging instruments and equipment
- Medical imaging subsystems
- Test and Measurement subsystems and systems
- Telecommunications
- High performance signal and imaging computation
- Commercial signal acquisition, measurement, and control

Organization and Culture

Analogic is organized to succeed. Using small, motivated, interdisciplinary design teams we have established an exceptional record for taking new ideas from concept to concrete reality in short periods. Our engineers have worked directly with virtually every type of transducer for measuring temperature, pressure, flow, weight, vibration, chemical parameters, mechanical position and condition, and velocity and acceleration.

To support further innovation and ensure reliable, well engineered solutions to technical challenges, Analogic has established a corporate culture and organizational framework that has repeatedly demonstrated its ability to deliver outstanding results.

ANALOGIC DIVISIONS & SUBSIDIARIES



Quality Manufacturing

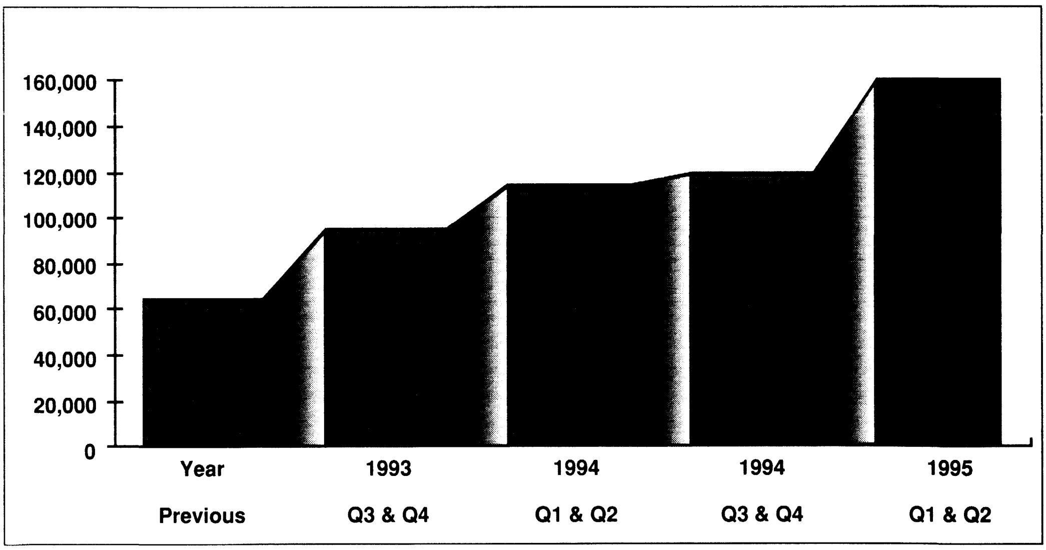
Key to Analogic's continued success is the ability to translate leading-edge designs into the highest quality finished products efficiently. Our large and modern manufacturing complex has the capacity, equipment and skilled production and testing personnel to produce many tens of thousands of custom units each month. Designing products with a competitive edge often means reducing size, power consumption and cost. Our in-house microelectronics manufacturing facility and surface mount capability provide our engineers with the processes required to address all three simultaneously.

Before being released to manufacturing, every Analogic design is subjected to worst case analysis. Our quality manufacturing begins with a unique in-house facility that screens critical components to our own performance and reliability requirements. In production, full sequence testing includes computerized testing of board-level sub-assemblies, and finished product is tested under asynchronous temperature and power cycling.

In 1994, Analogic began a comprehensive program to achieve Company-wide certification to ISO 9001, an internationally recognized quality system standard. All divisions, including our Data Conversion Products group, and two of our subsidiaries have been audited and certified. Over the years, Analogic products have consistently met safety and EMC standards of regulatory bodies worldwide, including: FDA, UL, NRC, CSA, and IEC.

CE 0197 **ISO 9001**

PRODUCT MEAN TIME BETWEEN FAILURE (MEDICAL DAS)



A Partial List of Converter-Related Patents

2,989,741	First Known Tracking A/D Converter and Digital Delta Modulator
2,997,704	First Known SR Program Successive Approximation Analog to Digital Converter
3,034,719	First Known Hybrid Analog/Digital Combined Analog/Digital Computing Link
3,054,910	First Known Differential Amplifier Comparator
3,108,266	First Known Current Switching Digital to Analog Converter
3,122,729	First Known Bipolar Dual Slope Ramp A/D Converter
3,588,881	First Known High-Precision Cyclic Analog/Digital Converter
3,611,354	First Known Series Shunt Multiplexing Switching System
3,649,924	First Known Sampling Amplifier
3,895,267	Modular Data Acquisition System Module

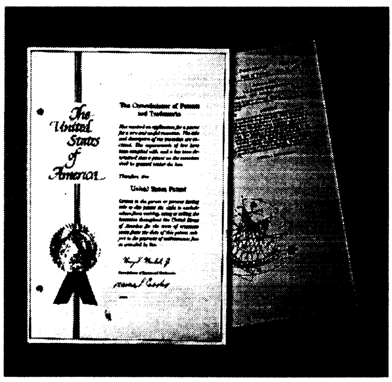


TABLE OF CONTENTS

Products Not Included in This Catalog

But Still Available

The products specified in this catalog represent the latest in high-performance, cost-effective devices available from Analogic today.

The products listed to the right have been designed into many applications in the past, but may no longer represent the most cost-effective solution to your new data acquisition needs. However, in the event that replacement parts are required, these products are still available. Pricing and data sheets are available upon request.

ADAM824B	14-bit, 20 kHz Sampling ADC
ADAM825B	15-bit, 20 kHz Sampling ADC
ADAM826 Series	16-Bit, 400 kHz Sampling ADCs
ADAM834B	14-bit, 20 kHz, Extended Temp. Sampling ADC
ADAM835B	15-bit, 20 kHz, Extended Temp. Sampling ADC
ADC3110M Series	14-bit, 2 MHz Sampling ADC
ADC3111M Series	14-bit, 2 MHz Sampling ADC
ADC4110	16-bit, 12.5 kHz Sampling ADC
ADC4111	16-bit, 12.5 kHz, Extended Temp. Sampling ADC
ADC4340	16-bit, 200 kHz Sampling ADC
ADC4342	16-bit, 400 kHz Sampling ADC
ADC4346M	16-bit, 400 kHz Sampling ADC
AH8308T	8-bit, 100 MHz Video DAC
AM30515	16-bit, 5 µs ADC
AM40316	16-bit, 200 kHz Sampling ADC
AM40516	16-bit, 125 kHz Sampling ADC
MP201A	Distortion Suppressor
MP260	S/H Amplifier, 5 µs to ±0.003%
MP271	S/H Amplifier, 1 µs to ±0.005%
MP1926A	16-bit Audio DAC
MP1936	16-bit Audio DAC with Distortion Suppressor
MP2321	Isolated, Integrating ADC with BCD Coding
MP2322	Isolated, Integrating ADC with Binary Coding
MP2734	14-bit, 6.8 µs ADC
MP2735A-1	15-bit, 125 kHz Sampling ADC
MP2735A-2	15-bit, 5 µs Buffered ADC
MP8016	16-bit, 32 µs ADC
MP8037	17-bit, 250 CPS Integrating ADC
MP8118	16-Bit DAC, ±1PPM/°C Absolute TC

Introduction and Technical Support

Both Before and After You Choose Your Data Conversion Product

Introduction

The purpose of this catalog is to provide you, the Data Conversion Products user, with an easy-to-use reference and selection guide for this line of Analogic products. Complete technical specifications are provided for all our products. These specifications assist the user in the selection of the appropriate product with respect to the most critical parameters for a given application.

This catalog contains most of our current standard Data Conversion products. However, we constantly have a number of products under development. If you do not locate a product in this catalog that meets your requirements, please contact your local sales representative.

For those applications where a standard product is not available or for those volume requirements where a customized product will provide a performance or price advantage, Analogic welcomes the opportunity to review those with you.

TECH SUPPORT

On-line Applications Support

Analogic is proud to offer our customers superior technical support, at NO CHARGE, both BEFORE and AFTER you choose your Data Conversion solution. Our Applications Engineers are extremely knowledgeable and can assist you in:

- ❑ Understanding Your Application Requirements
- ❑ Evaluating Your Specifications
- ❑ Selecting Signal Conditioning Modules
- ❑ Choosing the Proper Data Conversion Component
- ❑ Installing Applications
- ❑ Troubleshooting and Problem Solving
- ❑ Providing Total Systems Solutions

ORDERING AND CUSTOMER SERVICE

To place an order, call our toll-free number, your regional domestic sales office, or your local representative. Orders may be placed by mail, telephone or FAX. Telephone and FAX orders must be confirmed with a written purchase order. All orders should include model numbers, product description, option description, pricing, and billing and shipping addresses, as well as method of shipment.

International

Place International orders with an Analogic International Sales Rep. Orders received directly are deemed to be placed with our International sales representative. In countries without an Analogic representative, place orders directly by FAX and confirm by air mail.

Sales Representatives

Analogic employs field sales representatives throughout the United States, Canada, Europe, and the Far East. Only these sales representatives are authorized by Analogic to solicit sales, and any information received by other than authorized reps of Analogic or the factory are not considered binding upon Analogic.

Prices

All prices are F.O.B. Wakefield, MA USA in US Dollars. Applicable federal, state and local taxes are paid by the buyer.

Terms

Net 30 days. Consult factory for International terms.

Discounts

Quantity discounts are available per individual order. OEM discounts are also available on an order or contract basis. Consult the factory for details.

Quotations

Price and delivery quotations made by Analogic or its authorized sales representatives are valid for 30 days unless otherwise specified.

Delivery

Analogic ships all products in suitable commercial containers under normal conditions. Best available method of shipping will be used unless method is specified. Shipping charges, except Air Freight (sent collect), are prepaid and billed to customer.

Order Cancellation

All orders entered with Analogic are binding and subject to a cancellation charge if cancelled before or after the scheduled shipping date appearing on the acknowledgement.

Warranty

Analogic products are warranteed for a period of one year under Standard Warranty Terms.

Returns

All returns, in or out of warranty, must have a RMA (Return Material Authorization) number. Call Analogic for authorization. For returns outside the USA, contact your local field representative or Analogic directly for an RMA.

Repair Returns

Simply call our Customer Service Department at (508) 977-3000, Ext. 3617 (FAX 508-532-8913).

The effective date supersedes all other agreed upon dates unless specified otherwise.

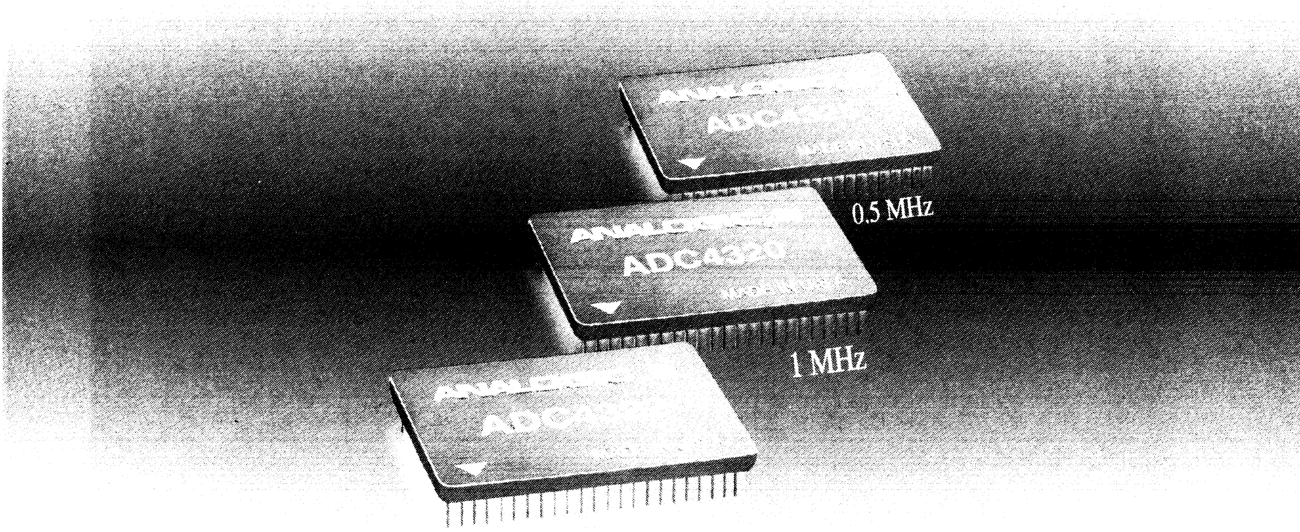
Prices subject to change without notice.

Analogic Corporation
Data Conversion Products Group
360 Audubon Road • Wakefield, MA 01880-9863, USA
Tel: (508) 977-3000 • Fax: (617) 245-1274 • Technical support: (800) 446-8936

European Sales Centre
Analogic Ltd.
Ascot House • Doncastle Road • Bracknell, Berks. RG12 8PE • England
Tel: +44-1344-860111 • Fax: +44-1344-860478

New Products from the Data Conversion Products Group

*The **Only** Pin-for-Pin Family of High Speed, 16-Bit A/D Converters Available Today!*



ADC4322	2 MHz	81 dB @ 980 kHz	86 dB	2.1W
ADC4320	1 MHz	84 dB @ 495 kHZ	89 dB	2.1W
ADC4325	500 kHz	92 dB @ 100 kHZ	91 dB	2.1W

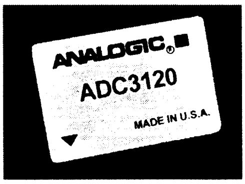
Call 1 (800) 446-8936

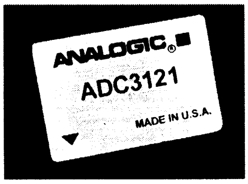
New Products from the Data Conversion Products Group

ADC3120

14-Bit, 20 Mz, Sampling A/D Converter

- 90 dB spurious free dynamic range
- 75 dB signal-to-noise ratio
- 46-pin hybrid package





ADC3121

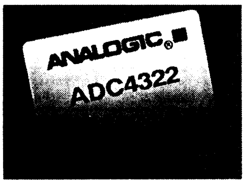
14-Bit, 20 Mz, Sampling A/D Converter

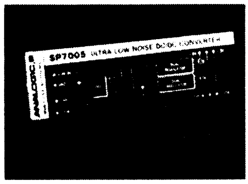
- 81 dB spurious free dynamic range
- 72 dB signal-to-noise ratio
- 46-pin hybrid package

ADC4322

16-Bit, 2 Mz, Sampling A/D Converter

- Pin-programmable input ranges
- 86 dB signal-to-noise ratio
- Low power 2.1W
- 81 dB @ 980 kHz





SP7005

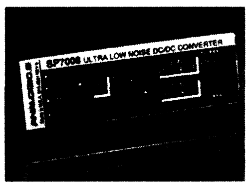
Quad Output DC-to-DC Converter

- +5V input
- ±15V, +5V, & -6V outputs
- 6 Watts
- Low noise plus ripple –5 mV P-P

ADC4320

16-Bit, 1 Mz, Sampling A/D Converter

- Pin-programmable input ranges
- 89 dB signal-to-noise ratio
- Low power 2.1W
- 84 dB @ 490 kHz



SP7008

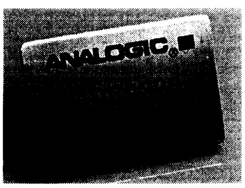
Quad Output DC-to-DC Converter

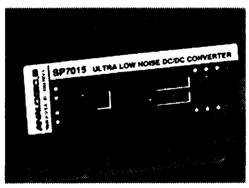
- +5V input
- ±15V, +5V, & -5V outputs
- 6 Watts
- Low noise plus ripple –5 mV P-P

ADC4325

16-Bit, 500 kHz, Sampling A/D Converter

- Pin-programmable input ranges
- 91 dB signal-to-noise ratio
- Low power 2.1W
- 92 dB @ 100 kHz





SP7015

Triple Output DC-to-DC Converter

- +5V input
- ±15V & +5V outputs
- 6.75 Watts
- Low noise plus ripple –5 mV P-P

ANALOGIC®
The World Resource for Precision Signal Technology

Sampling Analog-to-Digital Converters

Selection Guide

Model	Resolution	Speed	SNR	SFDR	Page
ADC5020/30	18 Bits	144 kHz	100 dB	110 dB	19
ADC4320	16 Bits	1 MHz	89 dB	97 dB	25
ADC4322	16 Bits	2 MHz	86 dB	97 dB	25
ADC4325	16 Bits	500 kHz	91 dB	97 dB	25
ADC4344	16 Bits	1 MHz	89 dB	99 dB	33
ADC4345	16 Bits	500 kHz	92 dB	99 dB	33
ADC4355/56	16 Bits	100 kHz	92 dB	110 dB	39
ADC4357	16 Bits	200 kHz	86 dB	100 dB	39
ADC3120	14 Bits	20 MHz	75 dB	90 dB	47
ADC3121	14 Bits	20 MHz	72 dB	81 dB	51
ADC3214	14 Bits	1MHz	76 dB	95 dB	55

Sampling A/D Converters

Glossary of Terms

Peak Distortion

The ratio, expressed in dB, between the RMS value of the highest spurious spectral component below the Nyquist rate and the RMS value of the signal.

$$\text{Peak Distortion} = 20 \log \frac{\text{RMS value max. spurious component}}{\text{RMS value of input signal}}$$

Signal to Noise Ratio

The ratio, expressed in dB, between the RMS value of the signal and the total RMS noise below the Nyquist rate. Note that all frequency bins that are correlated with the test frequency are removed and replaced with an average of the remaining bins

Total Harmonic Distortion

The ratio, expressed in dB, between the RMS sum of all harmonics up to the 100th harmonic and the RMS value of the signal. The components of this specification include both Direct and Reflected Harmonics.

Direct Harmonic Distortion

The ratio, expressed in dB, between the RMS sum of all the components below the Nyquist rate that are harmonically related to the signal and the RMS value of the signal.

Reflected Harmonic Distortion

The ratio, expressed in dB, between the RMS sum of all aliased harmonics and the RMS value of the signal. Aliased harmonics are those that "fold back" below the Nyquist frequency.

Note that the estimated RMS noise, based on those frequency bins not correlated with the test signal, is first removed from the harmonic frequency bins before the above distortion values are calculated.

High Speed, High Resolution Performance Testing

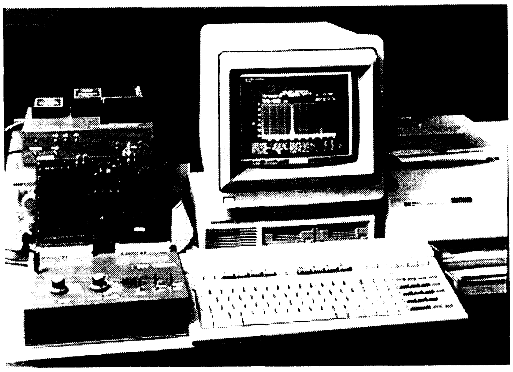
Technical Note

Introduction

To further instill confidence in our customers, Analogic supplies a test data sheet with each analog-to-digital (A/D) converter as proof of 100% testing performed on each device prior to shipping. Such data sheets reflect testing performed both in the "Frequency Domain" and in the "Amplitude Domain." The methods of testing A/D converters have developed significantly over the past decade to keep pace with the increased precision and speed of these converters. Not only have more of the testing methods become automated, but the demands on this automatic test equipment have increased significantly to test 16- to 18-bit performance fully in both the "Amplitude Domain" and the "Frequency Domain". In particular, testing A/D converters in the frequency domain has become a critical issue for many applications.

Analogic, one of the world leaders in data conversion technology, has developed automatic test systems for testing its family of 16- to 18-bit A/D converters in the amplitude and frequency domains. These testers were designed in conjunction with our engineering development effort on Analogic's family of high speed, high resolution A/D converters, since these converters perform beyond the testing capability of commercially available testers. Analogic's testers are used to perform a rigorous and exhaustive set of tests on each and every unit shipped by Analogic, assuring the customer that each unit meets or exceeds our published specifications.

At the present time, Analogic is one of the few manufacturers of A/D converters who fully specifies and tests its converters in the frequency domain. Other manufacturers provide one or two typical frequency domain specifications; Analogic provides a complete



set of frequency domain specifications. For applications such as professional audio or telecommunications, the frequency domain specifications are more significant than the amplitude domain specifications. Despite the importance of static testing, only frequency domain (dynamic) testing can completely delineate a converter's parametric performance in such demanding signal processing applications. Dynamic testing provides data for critical specifications for frequency domain applications; these specifications include total harmonic distortion, peak distortion, and signal to noise ratio. In addition, reflected harmonic distortion is an important parameter that few other A/D converter manufacturers provide, yet Analogic tests this parameter and prints the individual results on the frequency domain test data sheet.

In this technical note we provide the customer a view into Analogic's testing methodology, define our A/D converter parameters, and discuss in detail some of the critical issues in A/D converter testing.

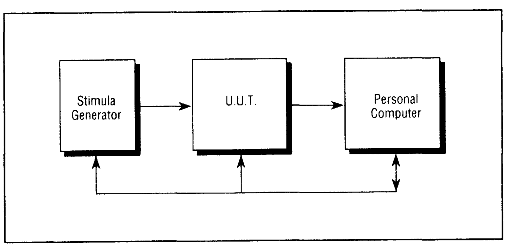
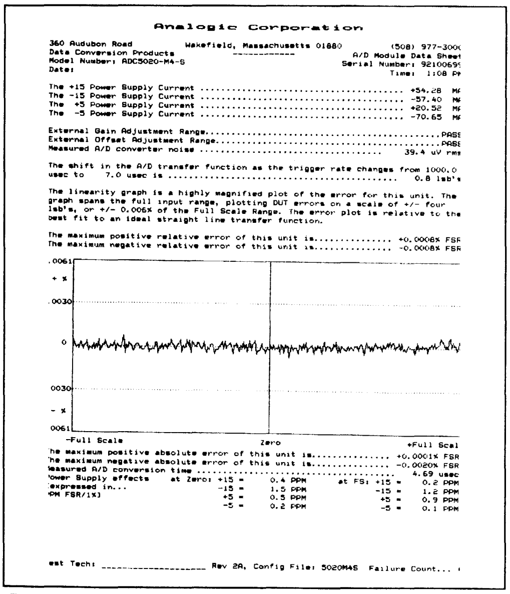


Figure 1. Amplitude Domain Test System.

Amplitude Domain Testing

Analogic's Amplitude Domain Test System, a simplified block diagram of which is shown in Figure 1, is controlled by a host computer and includes a 22-bit digital-to-analog converter, with accuracy and linearity far exceeding the requirements for testing 16- or 18-bit A/D converters. The reference for the D/A converter is traceable to the National Institute of Standards Technology. This degree of accuracy is essential for amplitude domain testing of A/D converters to the 18-bit level.

With this system, Analogic tests such parameters as integral linearity, dynamic differential linearity, A/D converter noise, conversion time, gain error, offset error, power supply current, and power supply rejection. The test system measures code transition voltages over the full range of the A/D converter and builds a histogram. Typical Amplitude Domain data sheet is shown in Figure 2.


Analogic Corporation

360 Audubon Road Wakefield, Massachusetts 01880 (508) 977-300(
Data Conversion Products A/D Module Data Sheet
Model Number: ADC5020-M4-S Serial Number: 9210069(
Date: Time: 1:08 P(

The +15 Power Supply Current .... +54.28 M(
The -15 Power Supply Current .... -57.40 M(
The +5 Power Supply Current .... +20.52 M(
The -5 Power Supply Current .... -70.65 M(

External Gain Adjustment Range.......... PAS(
External Offset Adjustment Range.......... PAS(
Measured A/D converter noise .... 39.4 uV rms

The shift in the A/D transfer function as the trigger rate changes from 1000.0 usec to 7.0 usec is .... 0.8 lsb's

The linearity graph is a highly magnified plot of the error for this unit. The graph spans the full input range, plotting DUT errors on a scale of +/- four lsb's, or +/- 0.006% of the Full Scale Range. The error plot is relative to the best fit to an ideal straight line transfer function.

The maximum positive relative error of this unit is.......... +0.0008% FSR
The maximum negative relative error of this unit is.......... -0.0008% FSR

(he maximum positive absolute error of this unit is.......... +0.0001% FSR
(he maximum negative absolute error of this unit is.......... -0.0020% FSR
(easured A/D conversion time .... 4.69 usec
(ower Supply effects at Zero: +15 = 0.4 PPM at FS: +15 = 0.2 PPM
(expressed in... -15 = 1.5 PPM -15 = 1.2 PPM
(PM FSR/1%] +5 = 0.5 PPM +5 = 0.9 PPM
-5 = 0.2 PPM -5 = 0.1 PPM

(est Tech: ____________ Rev 2A, Config File: 5020M4S Failure Count...

Figure 2. Typical Amplitude Domain Data Sheet.

Frequency Domain Testing

Many of the applications that use Analogic's high performance A/D converters, such as telecommunications, sonar and radar, require frequency domain test data.

A proprietary ADC spectral test station designed and manufactured by Analogic Corporation provides the frequency domain characterization for the sampling ADCs (see Figure 3). This test stations consists of a pair of low noise, low jitter, synthesized generators. One generator uses a narrow bandpass filter to create a clean input signal. The second generator, in conjunction with signal conditioning and an ECL Comparator, produces an extremely low jitter trigger signal. The need for a "windowing" algorithm is eliminated with a precise, coherent relationship between the two generators. This is critical in determining spectral characterization without the windowing side effects.

The resulting FFT data (See Figure 4 for the Test Data Sheet) is a spectral representation of the raw data generated by the test station and the device under test. It has not been massaged by a window function.

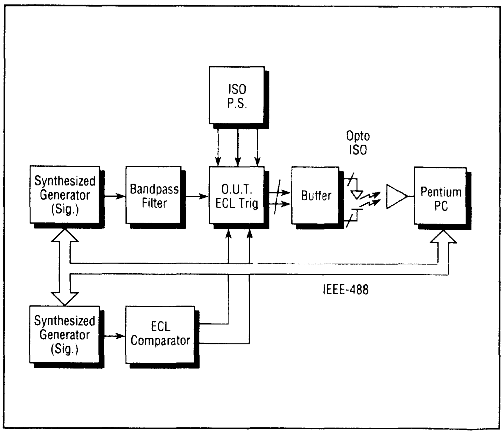


Figure 3. Frequency Domain Test System Block Diagram.

Spectral Analysis Test Data Sheet
Thursday, January 12, 1995, 11:06 AM

		Spurious Free Dynamic Range (a): 92.51 dB
ADC3120	Window: None	Actual Signal to Noise Ratio: 73.59 dB
20 MHz, 14 bit	Data Samples: 8192	Direct Harmonic Distortion: -92.70 dB
Serial Number:	FFT Averages: 16	Reflected Harmonic Distortion: -87.08 dB
	Signal Frequency: 3908691.4 Hz	Total Harmonic Distortion (THD): -85.75 dB
	Sampling Frequency: 20.0 MHz	S/N + Harmonic Distortion (SINAD): 73.29 dB

Legend

a:	Peak Distortion or Spurious Free Dynamic Range (SFDR)
b:	Average Noise Floor
Fo:	Analog Input Frequency
Fs:	Sampling Frequency
FSR:	Full Scale Input Voltage
FBW:	Analysis Bandwidth
FN:	Nyquist Frequency (Fs/2)
F2:	Second Harmonic (Direct)
F3-F10:	Reflected Harmonics (see note)
n:	Bits of Resolution
N:	Data Samples
P:	Period of Fo
V:	Actual Input Voltage Amplitude

Note:

Direct Harmonics are direct multiples of the fundamental input frequency and fall within the analysis bandwidth which is usually Nyquist.

Reflected Harmonics, or Aliased Harmonics, are direct multiples of the fundamental input frequency but fall outside of the Nyquist analysis bandwidth and are reflected back into the analysis bandwidth by mixing with the sampling frequency. An example in the FFT plot to the left is F3. (F3 = Fs − 3 • Fo)

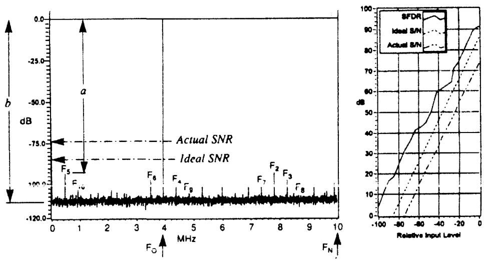


Figure 4. Spectral Analysis Test Data Sheet.

Windowing

One of the problems encountered in frequency domain testing is that a theoretically infinite-duration response must be truncated to a finite number of samples before the FFT is performed. This truncation process is called "windowing," and the selection of the appropriate window is critical to A/D testing.

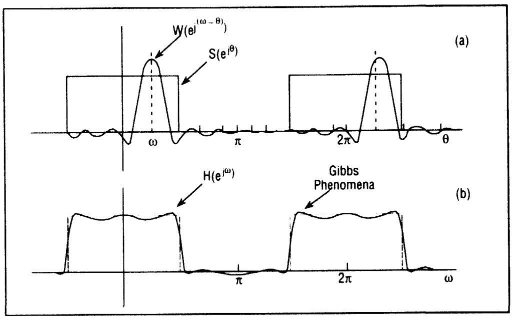


Figure 5. (a) Convolution Process Implied by Windowing. (b) Typical Approximation Resulting from Windowing.

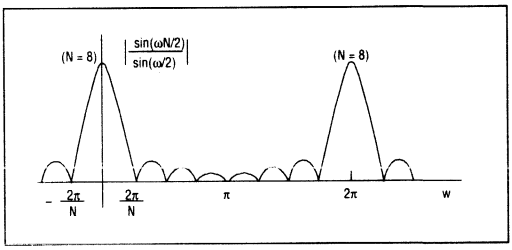


Figure 6. Magnitude of the Fourier Transform of a Rectangular Window (N = 8).

Intuitively, the "ideal" window, w(n), would seem to be a rectangular window of magnitude 1 and duration N, such that when it is multiplied in the time domain by the sampled data, s(n), the result, h(n), is:

$h(n) = s(n)\,w(n)$ $\quad$ $s(n)$ = Sampled Data
$w(n)$ = Window

such that:

$$h(n) = \begin{cases} s(n) & 0 \le n \le N-1 \\ 0, & \text{otherwise} \end{cases} \qquad w(n) = \begin{cases} 1, & 0 \le n \le N-1 \\ 0, & \text{otherwise} \end{cases}$$

In the frequency domain, the frequency response of h(n), namely $H(e^{j\omega})$, is therefore the convolution of $S(e^{j\omega})$ and $W(e^{j\omega})$:

$$H(e^{j\omega}) = \left(\frac{1}{2\pi}\right)\int_{-\pi}^{\pi} S\left(e^{j\theta}\right) W\left(e^{j(\omega-\theta)}\right) d\theta$$

Figure 5a shows this convolution, and Figure 5b shows the resulting $H(e^{j\omega})$.

It is desirable to minimize N to reduce the time to perform the FFT; yet the frequency response of w(n), namely $W(e^{j\omega})$, must be kept narrow relative to $S(e^{j\omega})$ so that $H(e^{j\omega})$ will closely resemble $S(e^{j\omega})$. This latter requirement derives from the fact that in the limit as $W(e^{j\omega})$ approaches an impulse, the convolution of $S(e^{j\omega})$ and $W(e^{j\omega})$ becomes identical to $S(e^{j\omega})$.

Clearly, these are conflicting requirements. As N increases, the width of the "main lobe" decreases, thus achieving the narrow frequency response, but at the expense of more data points. Figure 6 shows a wide main lobe for 8 data points. Furthermore, as N increases and the width of the main lobe decreases, the magnitude of the main lobe and its side lobes increase, since the area remains constant. In fact, the side lobes are only –13 dB down from the main lobe. The result is a non-uniform convergence to $S(e^{j\omega})$, an effect known as the Gibbs phenomena (refer to Figure 5b). The frequency response appears as a "smeared" version of the actual frequency response of $S(e^{j\omega})$.

The solution is to truncate the time domain data less abruptly by using a tapered window function rather than an abrupt rectangular window. This is the main principle behind the Rosenfeld, Blackman-Harris, and Blackman windows. These three windows greatly reduce the side lobes, but at the expense of a wider main lobe. Refer to Table 1*.

Note that this discussion on windowing is described in more detail on pages 239-250 of Alan Oppenheim and Ronald Shafer's text *Digital Signal Processing.*

Rosenfeld Window

The standard window that Analogic applies in testing its high resolution A/D converters is a Rosenfeld window. The theoretical discussion of this window was presented in 1986 by Eric Rosenfeld of LTX Corporation in an IEEE paper called "DSP Measurement of Frequency".

Briefly, the Rosenfeld window is optimized to minimize side lobe energy. The Rosenfeld window contains three components: a DC component and two cosine components. The frequency of the first cosine component is equal to the Fourier frequency (the reciprocal of the time duration of the window); the frequency of the second cosine component is equal to twice the Fourier frequency.

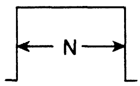
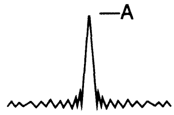
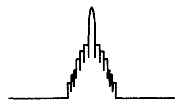
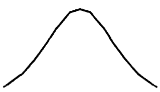
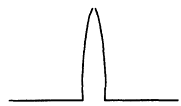
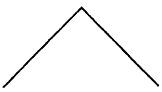
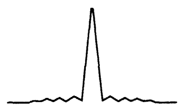
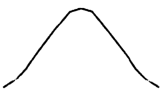
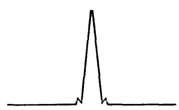
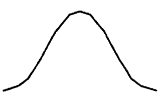
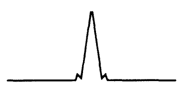
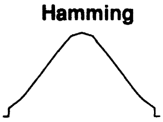
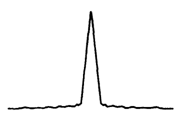
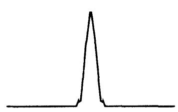
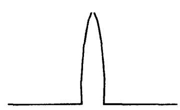
$$w(n) = (0.762 - \cos(2\pi n/N) + 0.238\cos(4\pi n/N)) / 1.05307$$

where: $\quad$ N = length of the window
$0 \le n \le N-1$

* Note: The table was comprised from the following sources:

1. "The FFT Fundamentals and Concepts" by Robert W. Ramirez.
2. "DSP Measurement of Frequency" by Eric Rosenfeld.
3. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform" by Fredric J. Harris.

Table 1. Some Common Windows and their Parameters.

Unity Amplitude Window	Shape Equation	Frequency Domain Magnitude	Major Lobe Height	Highest Side Lobe (dB)	Theoretical Roll-Off (dB/Octave)
Rectangle 	1 for n = 0 to N – 1		A	–13.2	6
Rosenfeld 	0.724 –0.950 cos 2 πn/N +0.226 cos 4 πn/N for n = 0 to N – 1		0.72A	–50	18
Blackman 	0.42 –0.50 cos 2 πn/N +0.08 cos 4 πn/N for n = –N/2 to (N/2) –1		0.42A	–58	18
Triangle 	2n/N for n = 0 to (N/2) – 1 –2n/N + 2 for n = N/2 to N – 1		0.5A	–26.7	12
Hanning 	0.5 (1 – cos 2 πn/N) for n = 0 to N – 1		0.5A	–31.6	18
Half Cycle Sine 	$\sin^3 2\pi\ 0.5\ n/N$ for n = 0 to N – 1		0.42A	–39.5	24
Hamming 	0.08 + 0.46 (1 – cos 2 πn/N) for n = 0 to N – 1		0.54A	–41.9	6
Cosine 	$(0.5\ (1 - \cos 2\ \pi n/N))^2$ for n = 0 to N – 1		0.36A	–46.9	30
Blackman-Harris 	0.42323 –0.49755 cos 2 πn/N +0.07922 cos 4 πn/N for n = 0 to N – 1		0.42A	–67	6

ADC5020/ADC5030

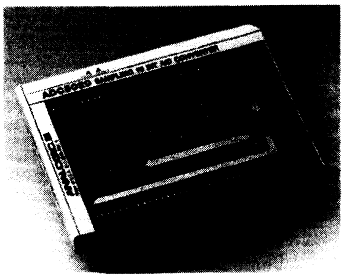
Wide Dynamic Range, High-Speed, 18-Bit Sampling A/D Converters

With Sub-ranging Architecture

Introduction

The ADC5020/ADC5030 18-bit A/D converter, designed with a unique sub-ranging architecture, achieves excellent speed, accuracy, and linearity. For digitizing fast time-varying signals, the ADC5020 has a built-in sample-and-hold amplifier. For applications with multiplexed DC signals or an external sample-and-hold, the more economical ADC5030 is available with a high impedance input buffer in place of the sample-and-hold. With a 144 kHz sampling rate, the ADC5020 can digitize professional audio signals (20 Hz to 20 kHz) at 3X oversampling, minimizing the design complexity of the anti-aliasing filters. The high sampling rate, low noise, low distortion and superior zero-crossing linearity of the ADC5020 optimize this converter for professional audio and spectroscopic applications.

The ADC5020/ADC5030's sub-ranging architecture uses a three-pass recycling technique in a design that both minimizes parts count and yields unprecedented stability, linearity, and accuracy. To achieve this superior performance, the ADC5020/ADC5030 relies on a proprietary reference D/A converter that has inherent 18-bit accuracy and linearity. The D/A converter, in conjunction with logic circuitry in a specialized gate array, detects and corrects inaccuracies and linearity errors that could arise from the flash A/D converter and amplifier circuitry in the conversion path. For applications requiring fine offset and gain adjustments, the converter has provisions for dynamically setting these DC parameters. The ADC5020/ADC5030 also provides easily accessible offset-trim and gain-trim potentiometers. This truly unique product comes in a fully-shielded 3" x 4" module with 0.1" pin spacings for easy installation on printed circuit boards. The specifications of the ADC5020/ADC5030 are fully ensured by thorough, computer-controlled factory tests.



Features

- ❑ 18-Bit Resolution
- ❑ 5 μs Conversion Time (ADC5030)
- ❑ 144 kHz Throughput Rate (ADC5020)
- ❑ No Missing Codes
- ❑ Wide Dynamic Range: 108 dB
- ❑ Signal-to-Noise Ratio: 105 dB (1 kHz)
- ❑ Peak Distortion: −110 dB (1 kHz)
- ❑ Total Harmonic Distortion: −105 dB (1 kHz)
- ❑ Ease of Use
- ❑ Built-in S/H Amplifier (ADC5020)
- ❑ TTL Compatibility
- ❑ Low Cost
- ❑ Low Power
- ❑ Electromagnetic/Electrostatic Shielding

Applications

- ❑ Professional Audio Encoding
- ❑ Spectroscopy
- ❑ Digital Telecommunications
- ❑ Automatic Test Equipment
- ❑ High-Resolution Imaging
- ❑ Seismic Instrumentation
- ❑ Medical Data Acquisition
- ❑ Satellite Communications
- ❑ Multiplexed Data Acquisition

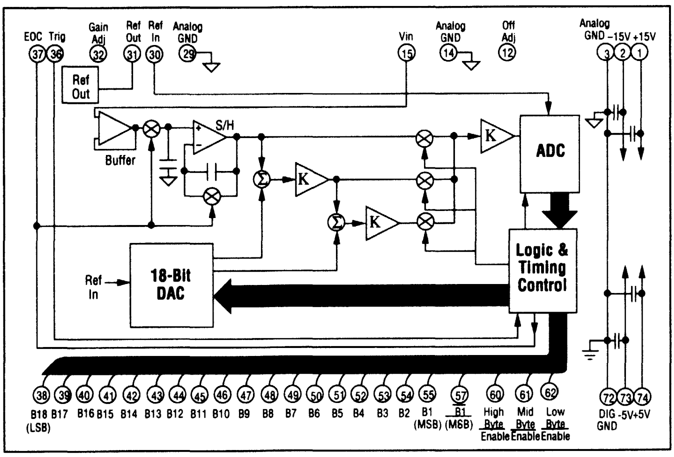


Figure 1. ADC5020 Functional Block Diagram.

ANALOGIC®
The World Resource for Precision Signal Technology

ANALOG INPUT

Input Range
±10V, ±5V, 0 to +10V (12)

Input Bias Current
500 nA Typ.

Input Capacitance
10 pF Typ.

Input Impedance
100 kΩ Typ.

DIGITAL INPUTS

Logic Levels
Logic "0"
0.8V Max.

Logic "1"
2.0V Min.

Logic Currents
Logic "0"
–0.4 mA

Logic "1"
20 μA

Trigger Pulse Width
50 ns Min.

High Byte Enable
Active Low B1-B8, B1

Mid Byte Enable
Active Low B9-B16

Low Byte Enable
Active Low B17, B18

DIGITAL OUTPUTS

Fan-Out
1 TTL Load Max.

Output Coding (12)
Offset Binary, Complementary Offset Binary, Two's Complement, Binary, Complementary Binary

Output Voltage
Logic "0"
0.4V Max.

Logic "1"
2.4V Min.

End of Conversion (EOC)
High During Conversion

REFERENCE

Internal Reference Output Voltage
–6.5V Typ. (1 mA DC external load)

Recommended Input (2)
–6.5V

Input Impedance
1.6 kΩ Typ.

DYNAMIC CHARACTERISTICS

Maximum Throughput Rate
ADC5020
144 kHz Min.

ADC5030
200 kHz Min.

A/D Conversion Time
5 Ms Max.

Signal-to-Noise Ratio (3, 6, 7)
DC to 10 kHz
105 dB Typ. 100 dB Min.

Peak Distortion (4, 6, 7)
1 kHz
–110 dB Typ., –100 dB Min.

10 kHz
–105 dB Typ., –95 dB Min.

Total Harmonic Distortion (5, 6, 7)
1 kHz
–105 dB Typ., –96 dB Min.

10 kHz
–100 dB Typ., –92 dB Min.

S/H Acquisition
1.9 μs Typ.

S/H Aperture Delay
30 ns Typ., 60 ns Max.

S/H Aperture Jitter
0.2 ns Typ., 0.4 ns Max. RMS

S/H Feedthrough (8)
–100 dB Max.

TRANSFER CHARACTERISTICS

Resolution
18 bits

Quantization Error
±0.5 LSB

Integral Nonlinearity
0.002% FSR Max., 0.0005% FSR Typ.

Differential Nonlinearity
±0.5 LSB Typ., ±0.8 LSB Max.

Offset Error (9, 10)
±1 mV Max.

Gain Error (9, 10)
0.01% FSR Max.

No Missing codes
Guaranteed from 0°C to 60°C

A/D Converter Noise
40 μV RMS ADC5020 (11)
30 μV RMS ADC5030

STABILITY (0°C TO 60°C)

Differential Nonlinearity
±0.5 ppm FSR/°C Max.

Offset Voltage
±10 ppm FSR/°C Max.

Gain
±10 ppm FSR/°C Max.

Warm-Up Time
5 minutes Max.

Supply Rejection
Offset
±5 ppm FSR/% Typ.

Gain
±5 ppm FSR/% Typ.

POWER REQUIREMENTS (14)

Supply Range
±15V Supplies (13)
11.65V Min., 15.45V Max.

±5V Supplies
4.75V Min., 5.25V Max.

±15V Current Drain
ADC5020
52 mA Typ.

ADC5030
42 mA Typ.

+5V Current Drain
40 mA Typ.

–5V Current Drain
70 mA Typ.

Power Consumption
ADC5020
2.11W Typ.

ADC5030
1.96W Typ.

ENVIRONMENTAL & MECHANICAL

Temperature Range
Rated Performance
0°C to 60°C

Storage
–25°C to 80°C

Relative Humidity
0 to 85% Non-condensing up to 60°C

Dimensions
3" x 4" x 0.44"

Shielding
Electromagnetic 5 sides, Electrostatic 6 sides

Case Potential
Ground

Notes:

1. Unless otherwise noted, all specifications apply at 25°C. Supplies are ±15V and ±5V. Full scale range is ±5V.
2. Reference input is optional. If it is not used, Ref In must be jumpered to Ref Out.
3. Signal-to-Noise Ratio represents the ratio of the RMS value of the signal to the total RMS noise below the Nyquist rate. The total RMS noise is computed by: (1) summing the noise power in all frequency bins not correlated with the test signal; (2) estimating the total noise power contained in all harmonic frequency bins; and (3) computing the RMS noise from the sum of (1) and (2).
4. Peak Distortion represents the ratio of the highest spurious frequency component below the Nyquist rate to the signal. Note that in computing Peak Distortion the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 3.
5. Total Harmonic Distortion represents the ratio of the RMS sum of all harmonics up to the 100th harmonic to the RMS value of the signal. Note that in computing Total Harmonic Distortion the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 3.
6. Analysis bandwidth is DC to 20 kHz with 3.5V RMS input signal.
7. ADC5030 tested and guaranteed with Analogic's SHA2410 Sample-and-Hold.
8. Measured with 10V p-p at 25 kHz.
9. Refer to "Output Coding and Trim Procedure" for field adjustable gain and offset procedures.
10. With use of internal reference only.
11. Includes noise from S/H and A/D converter.
12. See Ordering Guide.
13. For 0 to 10V range (ADC5020/ADC5030-1) Min. supplies are ±14.55V.
14. Analogic highly recommends the use of linear power supplies with its high performance, high resolution A/D converters. However, if system requirements provide only a +5V supply and limited space, the use of the Analogic SP7008 DC-to-DC converter will provide a low noise solution which will not degrade the ADC5020/ADC5030 performance.

Specifications subject to change without notice.

ADC5020/ADC5030 SPECIFICATIONS

Output Coding and Trim Procedure

Figure 2 shows the output coding of the ADC5020/ADC5030 A/D converter. The symbol * in Figure 2 indicates a bit that is undergoing a 0/1 or 1/0 code transition at the indicated analog input voltage.

To trim the offset of the ADC5020/ADC5030, apply 19 µV to the analog input. Adjust the offset trim potentiometer such that the digital output corresponds to the truth table of Figure 2.

To trim the gain of the ADC5020/ADC5030, apply +4.999981V for the bipolar option or +9.999943V for the unipolar option. Adjust the gain trim potentiometer such that the digital output corresponds to the truth table of Figure 2.

In addition to the internal offset and gain potentiometers, provisions have been made to dynamically null out DC errors by use of external potentiometers or DACs. The ratio of A/D converter DC shift to the external control voltage is 500 µV/V. A 10V swing from a DAC on Pin 12 produces a 5 mV offset shift, a 10V swing on Pin 32 produces a 5 mV gain shift.

Truth Table

Input Voltage	Digital Outputs: Comp. Offset Binary MSB … LSB	Digital Outputs: Straight Offset Binary MSB … LSB
Bipolar		
5.000000V	0000000000000000	1111111111111111
4.999981V	000000000000000*	111111111111111*
4.999962V	0000000000000001	1111111111111110
+0.000038V	0111111111111111	1000000000000000
+0.000019V	***************	***************
0.000000V	1000000000000000	0111111111111111
−4.999924V	1111111111111110	0000000000000001
−4.999943V	111111111111111*	000000000000000*
−4.999962V	1111111111111111	0000000000000000
Unipolar		
9.999962V	0000000000000000	1111111111111111
9.999943V	000000000000000*	111111111111111*
9.999924V	0000000000000001	1111111111111110
+5.000000V	0111111111111111	1000000000000000
+4.999981V	***************	***************
+4.999962V	1000000000000000	0111111111111111
+0.000038V	1111111111111110	0000000000000001
+0.000019V	111111111111111*	000000000000000*
+0.000000V	1111111111111111	0000000000000000

Figure 2. Output Coding for the ADC5020/ADC5030.

Timing Considerations

The timing diagram in Figure 3 shows the timing characteristics of the ADC5020/ADC5030 A/D converter. Upon a low-to-high transition of the Trigger Input, the end of conversion (EOC) line also switches high. The EOC line in turn switches the internal sample-and-hold amplifier to Hold mode; the S/H amplifier remains in Hold mode for the 5 µs duration of the A/D conversion period. At the end of the 5 µs A/D conversion period, the EOC line goes low and switches the sample-and-hold amplifier to Sample mode. At the 144 kHz throughput rate shown in Figure 3, the sample-and-hold amplifier then has 1.9 µs to sample (acquire) a new signal level for the next conversion cycle. The TTL-level Trigger input should have a minimum pulse width of 50 ns. Note that the data for a given conversion cycle becomes valid approximately 20 ns before the respective high-to-low transition of the EOC line.

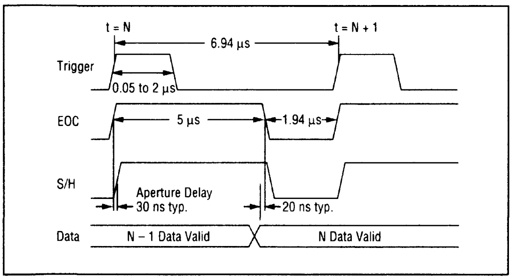


Figure 3. ADC5020/ADC5030 Timing Diagram.

Layout Considerations

Because of the ADC5020/ADC5030 A/D converter's extremely high resolution, it is necessary to pay careful attention to the printed circuit layout for the device. It is, for example, important to separate the analog and digital grounds and to return them separately to the system power supply. Digital grounds are often noisy or "glitchy", and these glitches can have adverse effects on the performance of the ADC5020/ADC5030 if they are introduced to the analog portions of the A/D converter's circuitry. At 18-bit resolution, the size of the voltage step between one code transition and the succeeding one is only 38 µV, so it is evident that any noise in the analog ground return can result in erroneous or missing codes. It is therefore important to configure a low-impedance ground-plane return on the printed circuit board. Note that the ground-potential metal case used for the ADC5020/ADC5030 provides shielding against electromagnetic interference on five sides and against electrostatic interference on six sides.

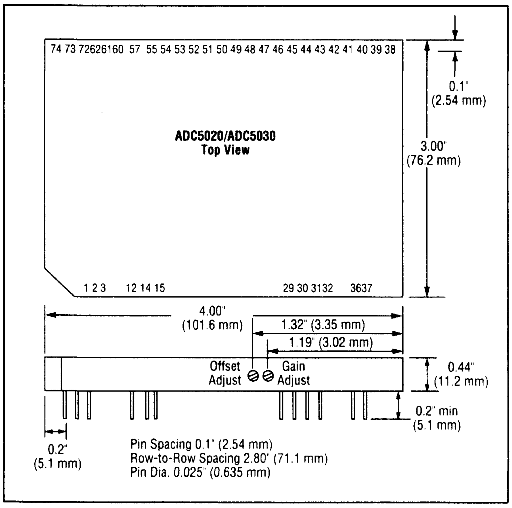


Figure 4. ADC5020/ADC5030 Outline Drawing & Pinouts.

PRINCIPLES OF OPERATION

To understand the operating principles of the ADC5020/ADC5030 A/D converter, refer to Figure 5. The simplified block diagrams in paths a, b, and c in Figure 5 illustrate the three successive passes in the sub-ranging conversion scheme of the ADC5020/ ADC5030. For all three passes, the lines labeled "From Input" come either from the output of the sample-and-hold amplifier (in the ADC5020) or from the output of the input buffer amplifier (in the ADC5030). All three passes use the same 8-bit flash A/D converter with the first and second pass utilizing only the first six bits. In the first pass (a), a switched-gain amplifier attenuates the input signal by a factor of five. It thus converts the 10V full scale range of the input to the 2V full scale range of the 6-bit flash A/D converter. The 6-bit A/D converter then digitizes the six MSBs of the input signal. The outputs of the A/D converter drive the six MSBs of the D/A converter. The six output lines of the A/D converter are actually latched into the logic circuitry of a specialized gate array, which drives the input lines of the D/A converter.

In the second pass (b), a difference amplifier subtracts the D/A converter's output voltage from the input voltage, then amplifies this difference by a factor of 3.2. The switched-gain amplifier now has a gain of two, and thus amplifies the difference voltage further. The output of the switched-gain amplifier again provides the input signal for the 8-bit flash A/D converter. The A/D converter's outputs are latched into the gate array which supplies the next lower-order bits of the D/A converter. In the gate array, the A/D converter's MSB in the second pass "overlaps" the LSB from the first pass. The resolution of the A/D conversion in the second pass is thus 11 bits (not 12).

In the third pass (c), the gain-of-3.2 difference amplifier subtracts the D/A converter's output voltage from the input voltage. In this pass, an amplifier with a gain of 32 provides additional amplification of the difference signal. The eight outputs of the 8-bit flash A/D converter are latched into the gate array; the MSB of this conversion cycle "overlaps" the LSB of the previous cycle. The effective resolution of the conversion is thus 6 + 5 + 7, or 18 bits. Using the "overlap" structure, logic circuitry in the gate array adds the digital words produced in the three passes and produces the corrected output word. This digital error-correction technique thus provides an output word that is accurate and linear to within the full resolution of the A/D converter. The method corrects for any gain and linearity errors in the amplifying circuitry, as well as in the 8-bit flash A/D

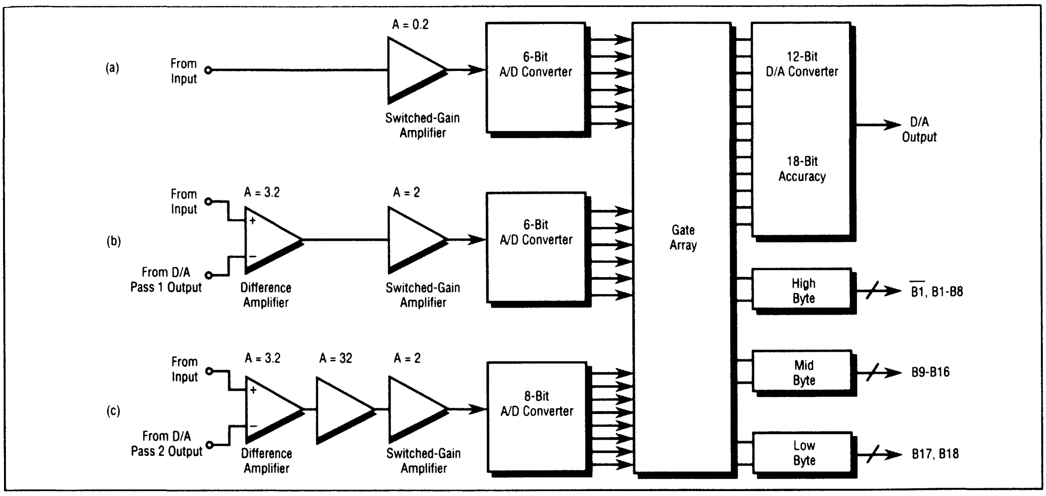


Figure 5. Operating Principle of the ADC5020/ADC5030.

converter. Without the error-correction technique, it would be necessary that all the components in the ADC5020/ ADC5030 — the difference amplifier, the switched-gain amplifier, and the 8-bit flash A/D converter — be accurate and linear to an 18-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve in production. The key to the ADC5020/ ADC5030's conversion scheme is the 18-bit-linear D/A converter, which serves as a reference element for the conversion passes as well as for the error-correction mechanism.

The ADC5020/ADC5030 has a tri-state output structure. Users can enable the eight MSBs, the eight middle bits, the two LSBs, or all bits by using the High-Byte Enable, Mid-Byte Enable, or the Low-Byte Enable pins (all three are active low). This feature makes it possible to transfer data from the ADC5020/ADC5030 to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered (see Figure 6).

TYPICAL APPLICATION

Figure 6 shows a typical application circuit for the ADC5020/ADC5030 A/D converter. This circuit provides simultaneous sampling for two professional audio analog-input channels. Simultaneous sampling is a necessity in conversion systems in which the phase, as well as amplitude relationship between different signals, is an important parameter. One example is in seismic measurements where it is crucial to know the phase relationship between the signals generated by different sensors. Another application where the phase and amplitude relationships are critical is professional digital audio, described in Figure 6. This application circuit performs simultaneous sampling by "freezing" the signal levels of both analog-input channels at the same instant of time. The amplitude relationship is maintained by the input Programmable Gain Amplifiers that are operated differentially to eliminate the possibility of errors arising from common mode voltages. The Anti-Aliasing Filters of Figure 6 reduce the out-of-band products coming in the front end that would mix with the sampling frequency and create audible in-band by-products.

A pair of low-noise, low-distortion Sample-and-Hold Amplifiers that have been optimized for audio bandwidths to obtain 18-bit linearity, Analogic's SHA2410s simultaneously sample the analog inputs and multiplex these signal levels to the buffer stage. A high input impedance buffer stage is required following a multiplexer to minimize the inherent nonlinearities of the switch-on-resistance with respect to current variations. The ADC5020 sequentially digitizes the two channels and transmits the buffered data to the minicomputer or microprocessor. The data buffer is necessary to prevent the coupling of high frequency noise from the processor bus into the A/D converters. Because the SHA2410s provide the sample-and-hold function in this circuit, the ADC5030, which does not include a sample-and-hold amplifier, is an appropriate choice.

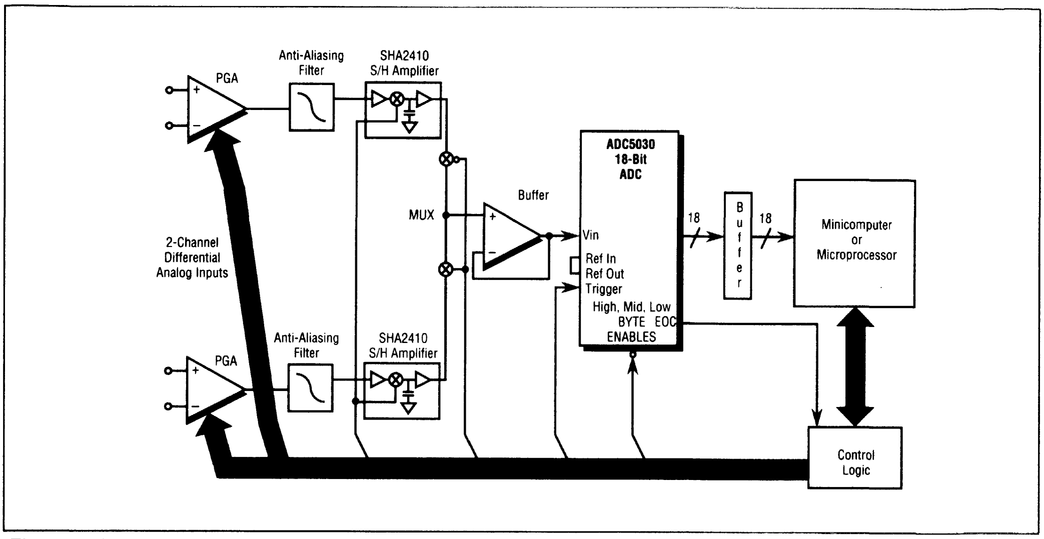


Figure 6. Typical Application Circuit for the ADC5030.

Ordering Guide

ADC50 __ -M __ __

20	On-board S/H	
30	Buffered input	
1	0 to +10V input	
2	±10V input	
4	±5V input	
S	Straight data	
C	Complementary data	
DC-to-DC Converter		**SP7008**

ADC4320/ADC4322/
ADC4325

Very High Speed 16-Bit, Sampling A/D Converters

in a Space-Saving 46-Pin Hybrid Package

Introduction

The ADC4320, ADC4322, and ADC4325 are complete 16-bit, 1 MHz, 2 MHz, and 500 kHz A/D converter subsystems with a built-in sample-and-hold amplifier in a space-saving 46-pin hybrid package. They offer pin-programmable input voltage ranges of ±2.5V, ±5V, ±10V and 0 to +10V, and have been designed for use in applications, such as ATE, digital oscilloscopes, medical imaging, radar, sonar, and analytical instrumentation, requiring high speed and high resolution front ends. The ADC4322 is capable of digitizing a 1 MHz signal at a 2 MHz sampling rate with a guarantee of no missing codes from 0°C to +70°C, or in an extended temperature range version, from –25°C to +85°C. Equally impressive in frequency domain applications, the ADC4325 features 91 dB minimum signal-to-noise ratio with input signals from DC to 100 kHz.

The ADC432X Series utilizes the latest semiconductor technologies to produce a cost-effective, high performance part in a 46-pin hybrid package. They are designed around a two-pass, sub-ranging architecture that integrates a low distortion sample-and-hold amplifier, precision voltage reference, ultra-stable 16-bit linear reference D/A converter, all necessary timing circuitry, and tri-state CMOS/TTL compatible output lines for ease of system integration.

Superior performance and ease-of-use make the ADC432X Series the ideal solution for those applications requiring a sample-and-hold amplifier directly at the input to the A/D converter. Having the S/H amplifier integrated with the A/D converter benefits the system designer in two ways. First, the S/H has been designed specifically to complement the performance of the A/D converter; for example, the acquisition time, hold mode settling and droop rate have been optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves

Continued on page 29.

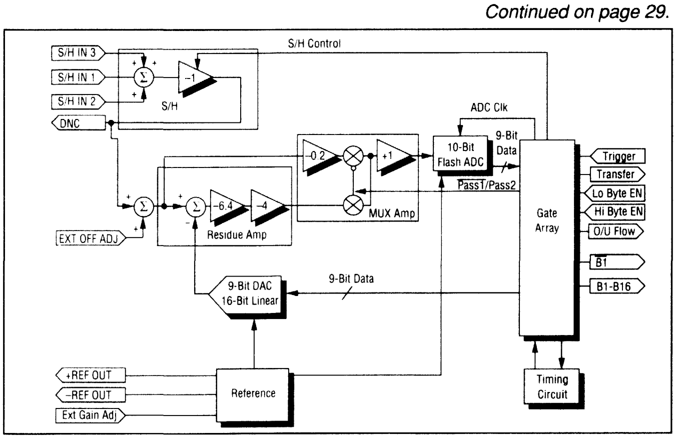
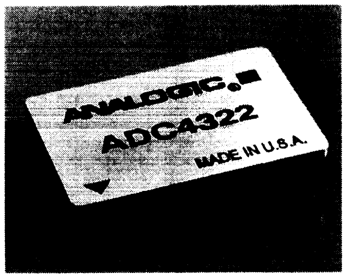


Figure 1. Functional Block Diagram.



Features

- ❑ 2 MHz, 1 MHz, and 500 kHz Conversion Rates
- ❑ 16-Bit Resolution
- ❑ 0.003% Maximum Integral Nonlinearity
- ❑ No Missing Codes
- ❑ Peak Distortion: –92 dB Max. (100 kHz Input)
- ❑ Signal to Noise Ratio:
  - 86 dB (ADC4322) Min.
  - 89 dB (ADC4320) Min.
  - 91 dB (ADC4325) Min.
- ❑ Total Harmonic Distortion: (100 kHz Input)
  - –86 dB (ADC4320) Max.
  - –90 dB (ADC4325) Max.
- ❑ TTL/CMOS Compatibility
- ❑ Low Noise
- ❑ Electromagnetic/Electrostatic Shielding

Applications

- ❑ Digital Signal Processing
- ❑ Sampling Oscilloscopes
- ❑ Automatic Test Equipment
- ❑ High-Resolution Imaging
- ❑ Analytical Instrumentation
- ❑ Medical Instrumentation
- ❑ CCD Detectors
- ❑ IR Imaging
- ❑ Sonar/Radar

SPECIFICATION	ADC4325	ADC4320	ADC4322
ANALOG INPUT			
Input Voltage Range			
Bipolar	±2.5V, ±5V, ±10V	±2.5V, ±5V, ±10V	±2.5V, ±5V, ±10V
Unipolar	0 to +10V	0 to +10V	0 to +10V
Max. Input Without Damage	±15.5V	±15.5V	±15.5V
Input Impedance			
±2.5V	750Ω	750Ω	750 Ω
±5.0V, 0-10V	1.5 KΩ	1.5 KΩ	1.5 KΩ
±10V	3 kΩ	3 kΩ	3 kΩ
Offset/Gain Adj. Sensitivity	300 ppm FSR/V	300 ppm FSR/V	300 ppm FSR/V
DIGITAL INPUTS			
Compatibility	TTL, HCT, and ACT	TTL, HCT, and ACT	TTL, HCT, and ACT
Logic "0"	+0.8V Max.	+0.8V Max.	+0.8V Max.
Logic "1"	+2.0V Min.	+2.0V Min.	+2.0V Min.
Trigger	Negative Edge Triggered	Negative Edge Triggered	Negative Edge Triggered
Loading	2 HCT Loads	2 HCT Loads	2 HCT Loads
TriggerPulse Width	100 ns Min.	100 ns Min.	50 ns Min.
High Byte $\overline{\text{Enable}}$	Active Low, B1-B8, $\overline{\text{B1}}$	Active Low, B1-B8, $\overline{\text{B1}}$	Active Low, B1-B8, $\overline{\text{B1}}$
Low Byte $\overline{\text{Enable}}$	Active Low, B9-B16	Active Low, B9-B16	Active Low, B9-B16
DIGITAL OUTPUTS			
Fan-Out	1 TTL Load	1 TTL Load	1 TTL Load
Logic "0"	+0.4V	+0.4V	+0.4V
Logic "1"	+2.4V	+2.4V	+2.4V
Output Coding	Binary, Offset Binary, Two's Complement	Binary, Offset Binary, Two's Complement	Binary, Offset Binary, Two's Complement
Transfer Pulse	Data valid on positive edge	Data valid on positive edge	Data valid on positive edge
Over/Under Flow	Valid = logic "0" (occurs only when ±FS have been exc'd.)	Valid = logic "0" (occurs only when ±FS have been exc'd)	Valid = logic "0" (occurs only when ±FS have been exc'd)
DYNAMIC CHARACTERISTICS[2]			
Maximum Throughput Rate	500 kHz	1.0 MHz	2.0 MHz
A/D Conversion Time	1.1 μs Typ.	620 ns Typ.	300 ns Typ.
S/H Acquisition Time	900 ns Typ.	380 ns Typ.	200 ns Typ.
S/H Aperture Delay	15 ns Max.	15 ns Max.	15 ns Max.
S/H Aperture Jitter	5 ps RMS Max.	5 ps RMS Max.	5 ps RMS Max.
S/H Feedthrough[3]	–90 dB Max.; –96 dB Typ.	–90 dB Max.; –96 dB Typ.	–90 dB Max.; –96 dB Typ.
Full Power Bandwidth	2.6 MHz Min.	3 MHz Min.	6 MHz Min.
Small Signal Bandwidth	2.6 MHz Min.	6 MHz Min.	8 MHz Min.
Signal to Noise Ratio[4]			
100 kHz Input @ 0 dB	91 dB Min.;93 dB Typ.	89 dB Min.; 92 dB Typ.	86 dB Min.; 88 dB Typ.
495 kHz Input @ –10 dB	–	79 dB Min.; 82 dB Typ.	76 dB Min.; 78 dB Typ.
980 kHz Input @ –10 dB	–	–	75 dB Min.; 78 dB Typ.
Peak Distortion[4]			
100 kHz Input @ 0 dB	–92 dB Max.; –97 dB Typ.	–92 dB Max.; –97 dB Typ.	–92 dB Max.; 97 dB Typ.
495 kHz Input @ –10 dB	–	–84 dB Max.; –95 dB Typ.	–84 dB Max.; –95 dB Typ.
980 kHz Input @ –10 dB	–	–	–81 dB Max.; –88 dB Typ.
Total Harmonic Distortion[4]			
100 kHz Input @ 0 dB	–90 dB Max.; –95 dB Typ.	–86 dB Max.; –94 dB Typ.	–86 dB Max. –94 dB Typ.
495 kHz Input @ –10 dB	–	–79 dB Max.; –86 dB Typ.	–80 dB Max.; –88 dB Typ.
980 kHz Input @ –10 dB	–	–	–80 dB Max.; –85 dB Typ.
THD + Noise[5]			
100 kHz Input @ 0 dB	88 dB Min.; 91 dB Typ.	84 dB Min.; 91 dB Typ.	83 dB Min.; 87 dB Typ.
495 kHz Input @ –10 dB	–	76 dB Min.; 81 dB Typ.	75 dB Min.; 77 dB Typ.
980 kHz Input @ –10 dB	–	–	74 dB Min.; 77dB Typ.

SPECIFICATION (CONT.)	ADC4325	ADC4320	ADC4322
Step Response[6]	800 ns Max. to 1 LSB	500 ns Max. to 1 LSB	250 ns Max. to 2 LSBs
INTERNAL REFERENCE[9]			
Voltage	+5V, ±0.5% Max.	+5V, ±0.5% Max.	+5V, ±0.5% Max.
Stability	15 ppm/°C Max.	15 ppm/°C Max.	15 ppm/°C Max.
Available Current[7]	1.0 mA Max.	1.0 mA Max.	1.0 mA Max.
TRANSFER CHARACTERISTICS			
Resolution	16 bits	16 bits	16 bits
Integral Nonlinearity	±0.003% FSR Max.; ±0.001% Typ.	±0.003% FSR Max.; ±0.001% Typ.	±0.003% FSR Max.; ±0.001% Typ
Differential Nonlinearity	±0.75 LSB; ±0.5 LSB Typ.	±0.75 LSB; ±0.5 LSB Typ.	±0.75 LSB Max.; ±0.5 LSB Typ.
Monotonicity	Guaranteed	Guaranteed	Guaranteed
No Missing Codes	Guaranteed over the Specified Temperature Range	Guaranteed over the Specified Temperature Range	Guaranteed over the Specified Temperature Range
Offset Error	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)
Gain Error	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)
Noise[8]			
10V p-p FSR	55 μV RMS Typ.; 70 μV RMS Max.	65 μV RMS Typ.; 80 μV RMS Max.	90 μV RMS Typ.; 110 μV Max.
5V p-p FSR	45 μV RMS Typ.; 55 μV RMS Max.	50 μV RMS Typ.; 60 μV RMS Max.	65 μV RMS Typ., 80 μV Max.
STABILITY			
Differential Nonlinearity TC	±1 PPM/°C MAX.	±1 PPM/°C MAX	.±1 PPM/°C MAX.
Offset TC	±15 ppm/°C Max.	±15 ppm/°C Max.	±15 ppm/°C Max.
Gain TC	±15 ppm/°C Max.	±15 ppm/°C Max.	±15 ppm/°C Max.
Warm-Up Time	5 Min. Max.	5 Min. Max.	5 Min. Max.
Supply Rejection per % change in any supply Offset & Gain	±10 ppm/% Max.	±10 ppm/% Max.	±10 ppm/% Max.
POWER REQUIREMENTS			
±15V Supplies[9]	14.55V Min., 15.45V Max.	14.55V Min., 15.45V Max.	14.55V Min., 15.45V Max.
+5V Supplies	+4.75V Min., +5.25V Max.	+4.75V Min., +5.25V Max.	+4.75V Min., +5.25V Max.
+15V Current Drain	63 mA Typ.	63 mA Typ.	71 mA Typ.
−15V Current Drain	54 mA Typ.	54 mA Typ.	61 mA Typ.
+5V Current Drain	67 mA Typ.	67 mA Typ.	67 mA Typ.
Total Power Consumption	2.1W Typ.	2.1W Typ.	2.3W Typ.
ENVIRONMENTAL & MECHANICAL			
Specified Temp. Range[10]			
A Version	0°C to +70°C	0°C to +70°C	0°C to +70°C
B Version	−25°C to +85°C	−25°C to +85°C	−25°C to +85°C
Storage Temp. Range	−25°C to 125°C	−25°C to 125°C	−25°C to 125°C
Dimensions	1.58" x 2.38" x 0.225" (40.13 mm x 60.45 mm x 5.7 mm)	1.58" x 2.38" x 0.225" (40.13 mm x 60.45 mm x 5.7 mm)	1.58" x 2.38" x 0.225" (40.13 mm x 60.45 mm x 5.7 mm)
Case Potential	Ground	Ground	Ground

NOTES:

1. All specifications guaranteed at 25°C unless otherwise noted and supplies at ±15V and +5V.
2. All dynamic characteristics measured on the ±5V input range except the 980 kHz distortion test are performed at the ±2.5V input range.
3. Measured with a full scale step input.
4. See performance testing.
5. THD + noise represents the ratio of the RMS value of the signal to the total RMS noise below the Nyquist plus the total harmonic distortion up to the 100th harmonic with an analysis bandwidth of DC to the converters' Nyquist frequency.
6. Step response represents the time required to achieve the specified accuracies after an input full scale step change.
7. Reference Load to remain stable.
8. Includes noise from S/H and A/D converter.
9. Both ±15V analog supply voltages and both ±reference voltages, Pins 2, 3, 16, and 17 must be by-passed with low ESR tantalum capacitors (see Figure 20).
10. The specified temperature range is guaranteed for the case temperature.

Specifications subject to change without notice.

TYPICAL PERFORMANCE CHARACTERISTICS

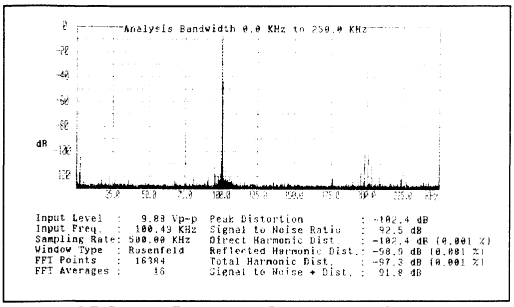


Fig. 2. ADC4325 Dynamic Characteristics at 100 kHz and 0 dB

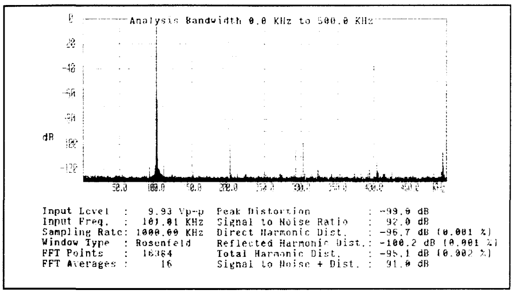


Fig. 3. ADC4320 Dynamic Characteristics at 100 kHz and 0 dB

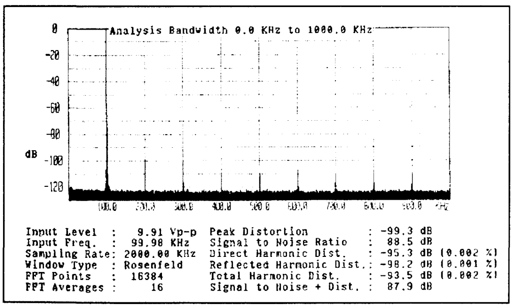


Fig. 4. ADC4322 Dynamic Characteristics at 100 kHz and 0 dB

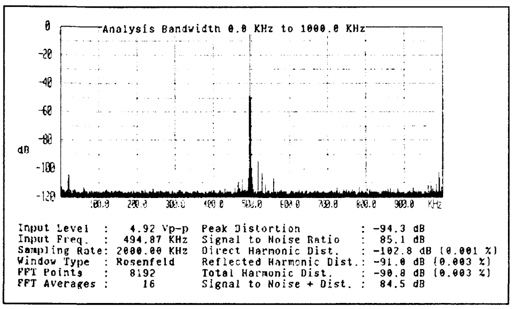


Fig. 5. ADC4322 Dynamic Characteristics at 495 kHz and 0 dB (±2.5V Range)

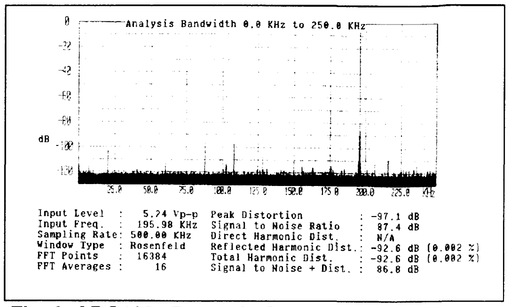


Fig. 6. ADC4325 Dynamic Characteristics at 195 kHz and –6 dB (±5V Range)

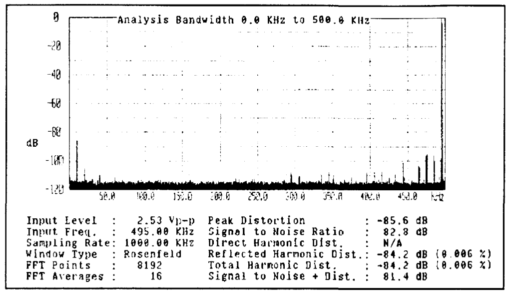


Fig. 7. ADC4320 Dynamic Characteristics at 495 kHz and –6 dB Range.

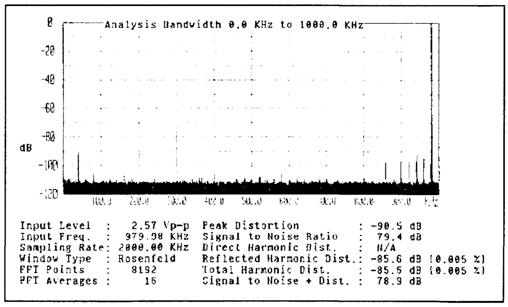


Fig. 8. ADC4322 Dynamic Characteristics at 980 kHz and –6 dB (±2.5V Range)

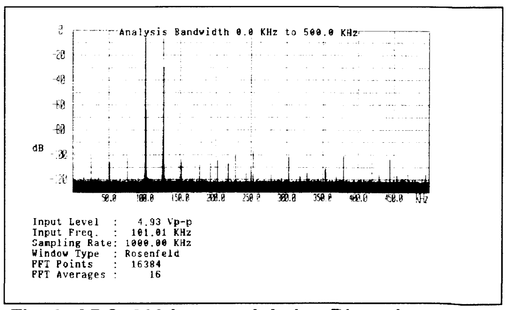


Fig. 9. ADC4320 Intermodulation Distortion at 100 kHz, 125 kHz and –6 dB

SPECIFICATIONS

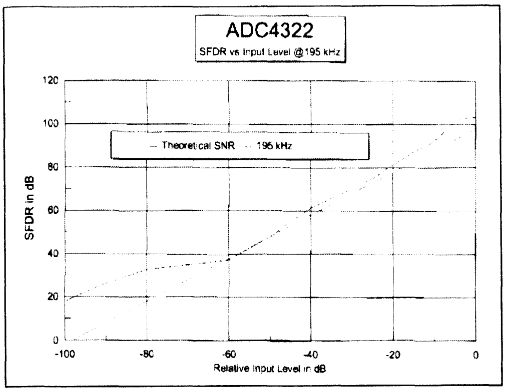


Figure 10. ADC4322 SFDR vs Input Level @ 195 kHz ±2.5V Range

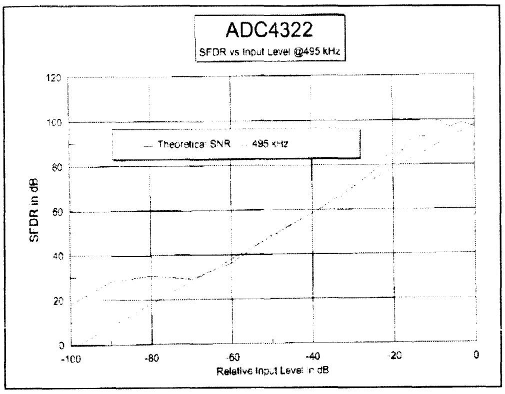


Figure 11. ADC4322 SFDR vs Input Level @ 495 kHz ±2.5V Range

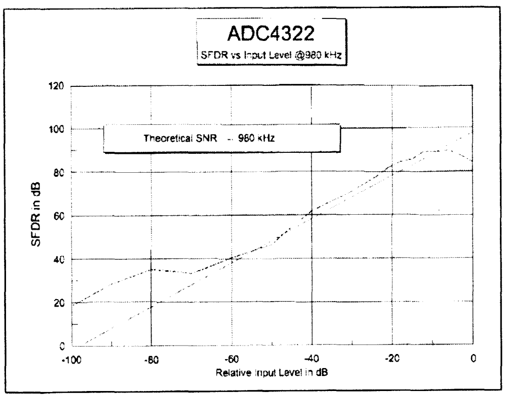


Figure 12. ADC4322 SFDR vs Input Level @ 980 kHz ±2.5V Range

PIN #	4	5	6
RANGE	S/H IN 1	S/H IN2	S/H IN 3
0V to +10V	Input	Input	–5V Ref
±5V	Input	Input	SIG RTN
±2.5V	Input	Input	Input
±10V	Input	SIG RTN	SIG RTN

Figure 13. Input Scaling Connections.

Continued from page 25.

true 16-bit performance, avoiding degradation due to ground loops, signal coupling, jitter and digital noise introduced when separate S/H and A/D converters are interconnected. Furthermore, the accuracy, speed, and quality of the ADC432X Series are fully ensured by thorough, computer-controlled factory tests of each unit.

INTERFACING

Input Scaling

The converters can be configured for four input voltage ranges: 0 to +10V; ±2.5V; ±5V; and ±10V. The analog input range should be scaled as close as possible to the maximum input to utilize the full dynamic range of the converter. Figure 13 describes the input connections.

Coding and Trim Procedure

Figure 15 shows the output coding and trim calibration voltages of the converter. For two's complement operation, simply use the available $\overline{B1}$ ($\overline{MSB}$) instead of B1 (MSB). Refer to Figure 14 for use of external offset and gain trim potentiometers. Voltage DACs with a ±5V output can be utilized easily when digital control is required. The input sensitivity of the external offset and gain control pins is 300 ppm FSR/V. If Offset and Gain adjusts are not used, connect them to Pin 14, Analog Returns.

To trim the offset of the converter, apply the offset voltage shown in Figure 15 for the appropriate voltage range. Adjust the offset trim potentiometer such that the 15 MSBs are "0" and the LSB alternates equally between "0" and "1" for the unipolar ranges or all 16 bits are in transition for the bipolar ranges.

To trim the gain of the converter, apply the range (+FS) voltage shown in Figure 15 for the appropriate range. Adjust the gain trim potentiometer such that the 15 MSBs are "1" and the LSB alternates equally between "0" and "1".

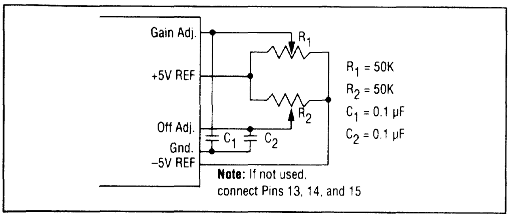


Figure 14. Offset and Gain Adjustment Circuit.

UNIPOLAR BINARY		0V TO +10V	
	MSB LSB		
+FS	111111111111111 *	= +9.99977V	
1/2 FS	1000000000000000	= +5.00000V	
Offset	000000000000000 *	= +0.00000V	
OFFSET BINARY		**±2.5V Input**	**±5V Input**
	MSB LSB		
+FS	111111111111111 *	= +2.49989V	+4.99977V
Offset	* * * * * * * * * * * * * * *	= –0.00004V	–0.00008V
–FS	000000000000000 *	= –2.49996V	–4.99992V
2'S COMPLEMENT		**±2.5V Input**	**±5V Input**
	MSB LSB		
+FS	011111111111111 *	= +2.49989V	+4.99977V
Offset	* * * * * * * * * * * * * * *	= –0.00004V	–0.00008V
–FS	100000000000000 *	= –2.49996V	–4.99992V

* denotes a 0/1 or 1/0 transition

Figure 15. Coding and Trim Calibration Table.

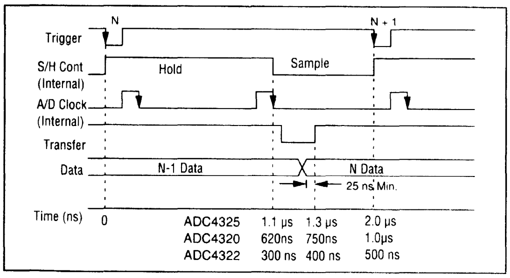


Figure 16. Timing Diagram.

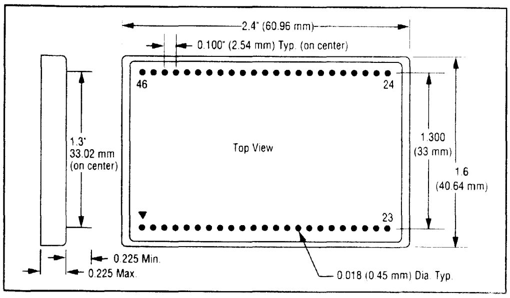


Figure 17. ADC432X Series Mechanical Diagram.

PIN #		PIN#	
1	ANA RTN	46	+5V
2	+15V	45	DIG RTN
3	–15V	44	O/U FLOW
4	S/H IN 1	43	BIT 1N
5	S/H IN 2	42	BIT 1
6	S/H IN 3	41	BIT 2
7	SIG RTN	40	BIT 3
8	DNC*	39	BIT 4
9	ANA RTN	38	BIT 5
10	+15V	37	BIT 6
11	–15V	36	BIT 7
12	DNC	35	BIT 8
13	EXT OFFSET ADJ	34	BIT 9
14	ANA RTN	33	BIT 10
15	EXT GAIN ADJ	32	BIT 11
16	+REF OUT	31	BIT 12
17	–REF OUT	30	BIT 13
18	ANA RTN	29	BIT 14
19	TRIGGER	28	BIT 15
20	DIG RTN	27	BIT 16
21	DIG RTN	26	TRANSFER
22	HI BYTE EN	25	+5V
23	LO BYTE EN	24	DIG RTN

* DNC– Do Not Connect

Figure 18. Pin Assignment.

To check the trim procedure, apply 1/2 full scale voltage for a unipolar range or –full scale voltage for the bipolar ranges and check that the digital code is ±1 LSB of the stated code.

PRINCIPLE OF OPERATION

The ADC432X Series converters are 16-bit sampling A/D converters with throughput rates of up to 2 MHz. These converters are available in three externally configured full scale ranges of 5V p-p, 10V p-p and 20V p-p. Options are externally or user-programmable for bipolar and unipolar inputs of ±2.5V, ±5V, ±10V and 0 to +10V. Two's complement format can be obtained by utilizing $\overline{B1}$ instead of B1.

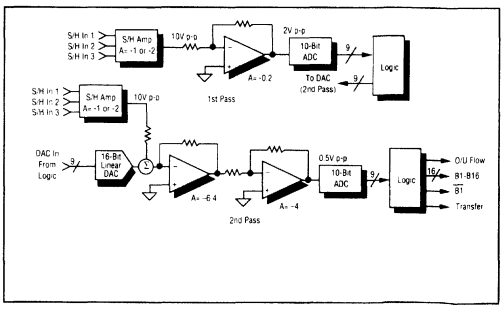


Figure 19. Operating Principle.

To understand the operating principles of the A/D converters, refer to the timing diagram of Figure 16 and the simplified block diagram of Figure 19. The simplified block diagram illustrates the two successive passes in the sub-ranging scheme of the converters.

The A/D converter is factory-trimmed and optimized to operate with a 10V p-p input voltage range. Scaling resistors at the S/H inputs configure the three input ranges and provide a S/H output voltage to the A/D converter of 10V p-p.

The first pass starts with a high-to-low transition of the trigger pulse. This signal places the S/H into the Hold mode and starts the timing logic. The path of the 10V p-p input signal during the first pass is through a 5:1 attenuator circuit to the 10-bit ADC with an input range of 2V p-p. At 35 ns, the ADC converts the signal and the 9 bits are latched both into the logic as the MSBs and into the 16-bit accurate DAC for the second pass.

The second pass subtracts the S/H output and the 9-bit, 16-bit accurate DAC output with the result equal to the 9-bit quantization error of the DAC, or 19.5 mV p-p. The "error" voltage is then amplified by a gain of 25.6 and is now 0.5V p-p or 1/4 the full scale range of the ADC, allowing a 2-bit overlap safety margin. When the DAC and the "error" amplifier have had sufficient time to settle to 16-bit accuracy, the amplified "error" voltage is then digitized by the ADC with the 9-bit second pass result latched into the logic. At this time the S/H returns to the sample mode to begin acquiring the next sample.

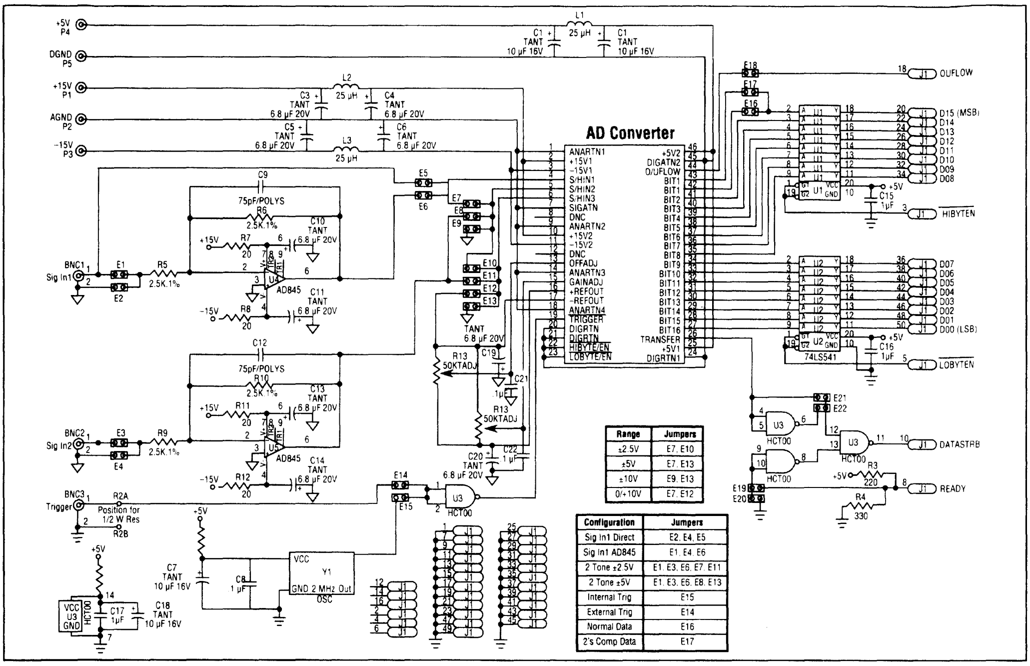
The 1/4 full scale range in the second pass produces a 2-bit overlap of the two passes. This provides an output word that is accurate and linear to 16 bits. This method corrects for any gain and linearity errors in the amplifying circuitry, as well as the 10-bit flash A/D converter. Without the use of this overlapping correction scheme, it would be necessary that all the components in the converters be accurate to the 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve on a production basis. The key to the conversion technique used in the converters is the 16-bit accurate and 16-bit linear D/A converter which serves as the reference element for the conversion's second pass. The use of proprietary sub-ranging architecture in the converters results in a sampling A/D converter that offers unprecedented speed and transfer characteristics at the 16-bit level.

The converter has a 3-state output structure. Users can enable the eight MSBs and B1 with $\overline{\text{HIBYTEN}}$ and the eight LSBs with $\overline{\text{LOBYTEN}}$ (both are active low). This feature makes it possible to transfer data from the converter to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered.

Layout Considerations

Because of the high resolution of the A/D converters, it is necessary to pay careful attention to the printed-circuit layout for the device. It is, for example, important to keep analog and digital grounds separate at the power supplies. Digital grounds are often noisy or "glitchy," and these glitches can have adverse effects on the performance of the converters if they are introduced to the analog portions of the A/D converter's circuitry. At 16-bit resolution, the size of the voltage step between one code transition and the succeeding one for a 5V full scale range is only 76 µV. It is evident that any noise in the analog ground return can result in erroneous or missing codes. It is important in the design of the PC board to configure a low-impedance ground-plane return on the printed-circuit board. It is only at this point where the analog and digital power returns should be made common.

The Analogic ADC4322 EB-1 evaluation board has been designed and laid out for optimum performance with the converter series. The board layout and schematic are shown in figures 20-22 as examples of decoupling and layout techniques.



Range	Jumpers
±2.5V	E7, E10
±5V	E7, E13
±10V	E9, E13
0/+10V	E7, E12

Configuration	Jumpers
Sig In1 Direct	E2, E4, E5
Sig In1 AD845	E1, E4, E6
2 Tone ±2.5V	E1, E3, E6, E7, E11
2 Tone ±5V	E1, E3, E6, E8, E13
Internal Trig	E15
External Trig	E14
Normal Data	E16
2's Comp Data	E17

Figure 20. ADC4322-EB1 Block Diagram

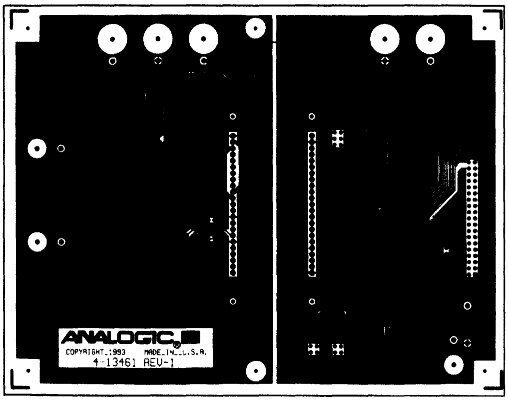


Figure 21. Primary Side

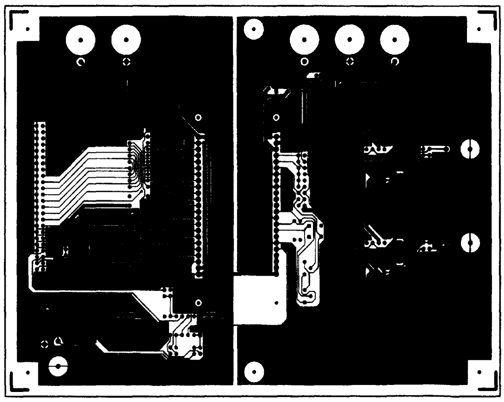


Figure 22. Secondary Side

Ordering Guide

Specified Temperature Range: 0°C to +70°C	
Model	**Sampling Rate**
ADC4325A	500 kHz
ADC4320A	1 MHz
ADC4322A	2 MHz
Specified Temperature Range: –25°C to +85°C	
ADC4325B	500 kHz
ADC4320B	1 MHz
ADC4322B	2 MHz
Evaluation Board	
ADC4322 EB-1	

Very High Speed, 16-Bit, 1 MHz and 500 kHz Sampling A/D Converters

With Built-in Sample-and-Hold Amplifiers

Description

The ADC4344 and ADC4345 are complete 16-bit, 1 MHz and 500 kHz A/D converter subsystems with a built-in sample-and-hold amplifier in a space-saving 2.5" x 3.5" x 0.44" package. They offer pin-programmable input voltage ranges of ±2.5V, ±5V and 0 to +10V. They are designed for use in applications requiring high speed and high resolution front ends such as ATE, digital oscilloscopes, medical imaging, radar, sonar, and analytical instrumentation. The ADC4344 is capable of digitizing a 500 kHz signal at a 1 MHz sampling rate with a guarantee of no missing codes from 0°C to +60°C. Equally impressive in frequency domain applications, the ADC4345 features 95 dB signal-to-noise ratio with input signals from DC to 100 kHz.

The ADC4344 and ADC4345 utilize the latest surface-mount technologies to produce a cost effective, high performance part in a 2.5" x 3.5" fully shielded package. They are designed around a two-pass, sub-ranging architecture that integrates a low distortion sample-and-hold amplifier, precision voltage reference, ultra-stable 16-bit linear reference D/A converter, all necessary timing circuitry and tri-state CMOS/TTL-compatible output lines for ease of system integration. The converters also offer an optional high-speed, low-noise input buffer for applications requiring high input impedance.

Continued on page 35.

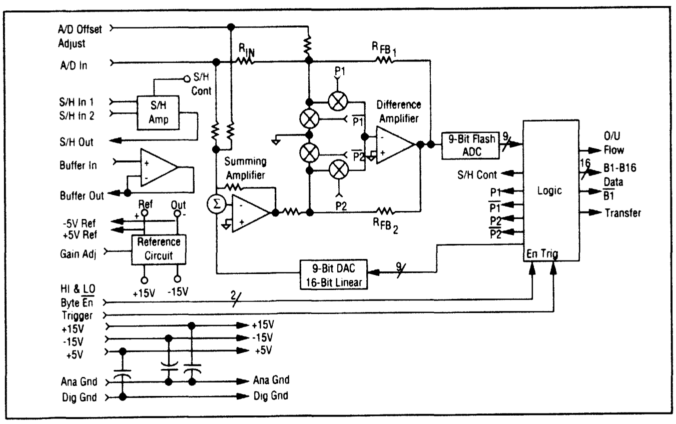
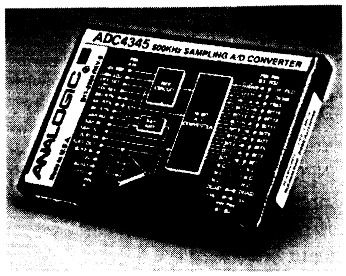


Figure 1. Functional Block Diagram.



Features

- ❑ Built-in S/H Amplifier
- ❑ Unique 2-Pass Sub-Ranging Architecture
- ❑ 16-Bit Resolution
- ❑ 1 MHz and 500 kHz Conversion Rate
- ❑ 0.003% Maximum Integral Nonlinearity
- ❑ No Missing Codes
- ❑ Peak Distortion: –99 dB (100 kHz Input)
- ❑ Signal to Noise Ratio: 100 kHz Input 92 dB, ADC4344; 95 dB, ADC4345
- ❑ Total Harmonic Distortion: –93 dB (100 kHz Input)
- ❑ TTL/CMOS Compatibility
- ❑ Low Noise
- ❑ Compact Size: 2.5" x 3.5" x 0.44"
- ❑ Electromagnetic/Electrostatic Shielding

Applications

- ❑ Digital Signal Processing
- ❑ Sampling Oscilloscopes
- ❑ Automatic Test Equipment
- ❑ High-Resolution Imaging
- ❑ Analytical Instrumentation
- ❑ Medical Instrumentation
- ❑ CCD Detectors
- ❑ IR Imaging
- ❑ Sonar
- ❑ Radar

ANALOG INPUT

Input Voltage Range
Bipolar
±2.5V, ±5V

Unipolar
0 to +10V

Max. Input Without Damage
±15.5V Typ.

S/H Direct Input Resistance
2.5 kΩ Typ.

Ext. Offset and Gain Adj. Sensitivity
2 mV/V

INPUT BUFFER [2]

Input Bias Current
10 nA Max.

Input Resistance
100 MΩ Typ.

Input Capacitance
10 pF Typ.

F.S. Settling Time
800 ns Typ. to 0.0015%

DIGITAL INPUTS

Compatibility
TTL, HCT, and ACT

Logic "0"
+0.8V Max.

Logic "1"
+2.0V Min.

Trigger
Positive Edge Triggered

Loading
1 TTL Load Min.

Pulse Width
100 ns Min.

High Byte $\overline{\text{Enable}}$
Active Low, B1-B8, $\overline{\text{B1}}$

Low Byte $\overline{\text{Enable}}$
Active Low, B9-B16

INTERNAL REFERENCE

Voltage
±5V, ±0.1% Max

Stability
10 ppm/°C Max.

Available Current [3]
0.5 mA Max.

DIGITAL OUTPUTS

Fan-Out
1 TTL Load

Logic "0"
+0.4V Max.

Logic "1"
+2.4V Min.

Output Coding
Binary, Offset Binary, 2's Comp.

Transfer Pulse
Data valid on positive edge

Over/Under Flow
Valid = logic "0" (occurs only when ±FS have been exceeded)

DYNAMIC CHARACTERISTICS [4]

Maximum Throughput Rate
500 kHz Min. (ADC4345)
1.0 MHz Min. ((ADC4344)

A/D Conversion Time
1.2 µs Typ. (ADC4345)
620 ns Typ. (ADC4344)

S/H Acquisition Time
800 ns Typ. (ADC4345)
380 ns Typ. (ADC4344)

S/H Aperture Delay
15 ns Max.

S/H Aperture Jitter
10 ps rms Max.

S/H Feedthrough [5]
–90 dB Max.; –96 dB Typ.

Full Power Bandwidth
1.5 MHz Min. (ADC4345)
3.0 MHz Min. (ADC4344

Small Signal Bandwidth
2.8 MHz Typ. (ADC34345)
4.0 MHz Typ. (ADC34344)

Slew Rate
50V/µs Typ. (ADC4345)
100V/µs Typ. (ADC4344)

Signal to Noise Ratio [6]
100 kHz input @ 0 dB
92 dB Min., 95 dB Typ. (ADC4345)
89 dB Min., 92 dB Typ. (ADC4344)

540 kHz input @ -10 dB (ADC4344)
79 dB Min., 82 dB Typ.

Peak Distortion[6]
100 kHz input @ 0 dB
–92 dB Max., –99 dB Typ.

@ –20 dB
–92 dB Typ.

540 kHz input @ -10 dB (ADC4344)
84 dB Min., 91 dB Typ.

Total Harmonic Distortion[6]
20 kHz input @ 0 dB
–90 dB Max., –97 dB Typ.

@ –20 dB
–82 dB Typ.

100 kHz input @ 0 dB
–86 dB Max., –93 dB Typ. (ADC4345)
–86 dB Max., –97 dB Typ. (ADC4344)

@ –20 dB
–82 dB Typ.

540 kHz input @ -10 dB (ADC4344)
–79 dB Min., –86 dB Typ.

THD + Noise[7]
20 kHz input @ 0 dB
89 dB Min., 92 dB Typ. (ADC4345)
87 dB Min., 90 dB Typ. (ADC4344)

@ –20 dB
75 dB Typ. (ADC4345)
72 dB Typ. (ADC4344)

100 kHz input @ 0 dB
86 dB Min., 91 dB Typ. (ADC4345)
84 dB Min., 89 dB Typ. (ADC4344)

@ –20 dB
75 dB Typ. (ADC4345)
72 dB Typ. (ADC4344)

540 kHz input @ -10 dB (ADC4344)
76 dB Min., 81 dB Typ.

Step Response[8]
800 ns Max. to 1 LSB

TRANSFER CHARACTERISTICS

Resolution
16 bits

Quantization Error
±0.5 LSB Max.

Integral Nonlinearity
±0.003% FSR Max.

Differential Nonlinearity
±0.75 LSB Max.

Monotonicity
Guaranteed

No Missing Codes
Guaranteed 0°C to +60°C

Offset Error
±0.1% FSR Max. (Adj. to Zero)

Gain Error
±0.1% FSR Max. (Adj. to Zero)

Noise w/o Buffer[9]
10V p-p FSR
50 µV rms Typ., 56 µV rms Max. (ADC4345)
70 µV rms Typ., 80 µV rms Max. (ADC4344)

5V p-p FSR
35 µV rms Typ., 40 µV rms Max. (ADC4345)
50 µV rms Typ., 55 µV rms Max. (ADC4344)

Noise including Buffer [9]
10V p-p FSR
56 μV rms Typ., 70 μV rms Max. (ADC4345)
79 μV rms Typ., 100 μV rms Max. (ADC4344)
5V p-p FSR
42 μV rms Typ., 50 μV rms Max. (ADC4345)
60 μV rms Typ., 70 μV rms Max. (ADC4344)

STABILITY (0°C TO 60°C)

Differential Nonlinearity TC
±1 ppm/°C Max.
Offset TC
±10 ppm/°C Max., ±5 ppm/°C Typ.
Gain TC
±10 ppm/°C Max., ±5 ppm/°C Typ.
Warm-Up Time
5 Min. Max.

Supply Rejection per % change in any supply
Offset
±10 ppm/% Max., ±2 ppm/% Typ.
Gain
±10 ppm/% Max., ±2 ppm/% Typ.

POWER REQUIREMENTS

±15V Supplies
14.55V Min., 15.45V Max.
+5V Supplies
+4.75V Min., +5.25V Max.
+15V Current Drain
100 mA Typ.
–15V Current Drain
100 mA Typ.
+5V Current Drain
80 mA Typ.
Total Power Consumption
3.4W Typ.

ENVIRONMENTAL & MECHANICAL

Specified Temp. Range
0°C to 60°C
Storage Temp. Range
–25°C to 80°C
Relative Humidity
85%, non-condensing to 60°C
Dimensions
2.5" x 3.5" x 0.44"
(63.5 x 88.9 x 11.18 mm)
Shielding
Electromagnetic 6 sides
Electrostatic 6 sides
Case Potential
Ground

NOTES

1. All specifications guaranteed at 25°C unless otherwise noted and supplies at ±15V and +5V.
2. The input buffer need only be used when a high impedance input is required.
3. Reference Load to remain stable during conversion.
4. Dynamic characteristics on ±5V input range and without input buffer unless otherwise noted.
5. Measured with a full scale step input with a 20V/μs rise time.
6. See performance testing.
7. THD + noise represents the ratio of the rms value of the signal to the total RMS noise below the Nyquist plus the total harmonic distortion up to the 100th harmonic with an analysis bandwidth of DC to the Nyquist rate.
8. Step response represents the time required to achieve the specified accuracies after an input full scale step change.
9. Includes noise from S/H and A/D converter.

Specifications subject to change without notice.

Continued from page 33.

Superior performance and ease-of-use of these converters make an ideal solution for those applications requiring a sample-and-hold amplifier directly at the input to the A/D converter. Having the S/H amplifier integrated with the A/D converter benefits the system designer in two ways. First, the S/H is designed specifically to complement the performance of the A/D converter; for example, the acquisition time, hold mode settling, and droop rate are optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves true 16-bit performance, avoiding degradation due to ground loops, signal coupling, jitter, and digital noise introduced when separate S/H and A/D converters are interconnected. Furthermore, the accuracy, speed, and quality of the ADC4344 and ADC4345 are fully ensured by thorough, computer-controlled factory tests of each unit.

SPECIFICATIONS

Input Scaling

The ADC4344 and ADC4345 can be configured for three input voltage ranges: 0 to +10V, ±2.5V, and ±5V. The Analog input range should be scaled as close as possible to the maximum input to utilize the full dynamic range of the converter. Figure 2 describes the input connections.

Pin#	A8	A9
Range	**S/H In 1**	**S/H In 2**
0V to +10V	Input	–5V Ref
±5V	Input	SIG RTN
±2.5V	Input	Input

Figure 2. Input Scaling Connections.

Coding and Trim Procedure

Figure 4 shows the output coding and trim calibration voltages of the A/D converter. For two's complement operation, simply use the available $\overline{\text{B1}}$ ($\overline{\text{MSB}}$) instead of B1 (MSB). Refer to Figure 3 for use of external offset and gain trim potentiometers. Voltage DACs with a ±10V output can be utilized easily when digital control is required. The input sensitivity of the external offset and gain control pins is 2 mV/V. If the external offset and gain adjust pins are not used, connect to Pin A12.

To trim the offset of the AD converter, apply the offset voltage shown in Figure 4 for the appropriate voltage range. Adjust the offset trim potentiometer such that the 15 MSBs are "0" and the LSB alternates equally between "0" and "1" for the unipolar ranges or all 16 bits are in transition for the bipolar ranges.

To trim the gain of the ADC4345, apply the range (+FS) voltage shown in Figure 4 for the appropriate range. Adjust the gain trim potentiometer such that the 15 MSBs are "1" and the LSB alternates equally between "0" and "1".

To check the trim procedure, apply 1/2 full scale voltage for a unipolar range or –full scale voltage for the bipolar ranges and check that the digital code is ±1 LSB of the stated code.

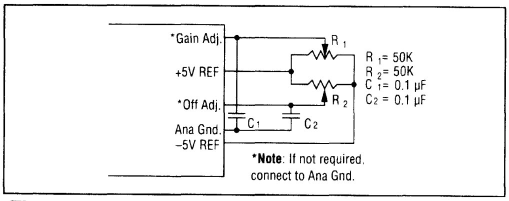


Figure 3. Offset and Gain Adjustment Circuit.

UNIPOLAR BINARY			0V TO +10V	
	MSB LSB			
+FS	111111111111111*	=	+9.99977V	
1/2 FS	1000000000000000	=	+5.00000V	
Offset	000000000000000*	=	+0.00008V	
OFFSET BINARY			**±2.5V input**	**±5V input**
	MSB LSB			
+FS	111111111111111*	=	+2.49989V	+4.99977V
Offset	***************	=	–0.00004V	–0.00008V
+FS	000000000000000*	=	–2.49996V	–4.99992V
2'S COMPLEMENT			**±2.5V input**	**±5V input**
	MSB LSB			
+FS	011111111111111*	=	+2.49989V	+4.99977V
Offset	***************	=	–0.00004V	–0.00008V
–FS	100000000000000*	=	–2.49996V	–4.99992V

Figure 4. Coding and Trim Calibration Table.

Layout Considerations

Because of the high resolution of the ADC4344/ ADC4345 A/D converters, it is necessary to pay careful attention to the printed-circuit layout for the device. It is, for example, important to return analog and digital grounds separately to their respective power supplies. Digital grounds are often noisy or "glitchy", and these glitches can have adverse effects on the performance of the ADC4345 if they are introduced to the analog portions of the A/D converter's circuitry. At 16-bit resolution, the size of the voltage step between one code transition and the succeeding one for a 5V full scale range is only 76 µV. It is evident that any noise in the analog ground return can result in erroneous or missing codes. It is important in the design of the PC board to configure a low-impedance ground-plane return on the printed-circuit board. It is only at this point, where the analog and digital power returns should be made common.

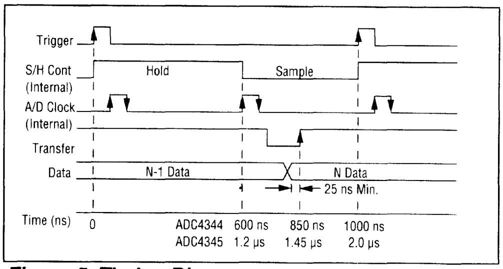


Figure 5. Timing Diagram.

PRINCIPLE OF OPERATION

The ADC4344 and ADC4345 are 16-bit sampling A/D converters with a throughput rate of up to 1 MHz. These converters are available in two externally configured full scale ranges of 5V p-p and 10V p-p. Both options are externally or user-programmable for bipolar and unipolar inputs of ±2.5V, ±5V and 0 to +10V. Two's complement format can be obtained by utilizing $\overline{\text{B1}}$ instead of B1.

To understand the operating principles of the A/D converter, refer to the timing diagram of Figure 5 and the simplified block diagram of Figure 6. The simplified block diagram illustrates the two successive passes in the sub-ranging scheme of the AD converter.

The A/D converter section of the converters is factory-trimmed and optimized to operate with a 10V p-p input

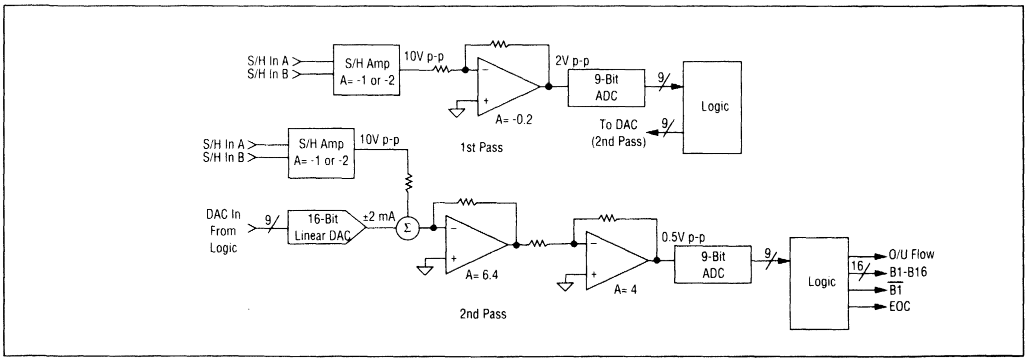


Figure 6. Operating Principle of the ADC4344 and ADC4345.

voltage range. Scaling resistors at the S/H inputs configure the three input ranges and provide a S/H output voltage to the A/D converter of 10V p-p.

The first pass starts with a low-to-high transition of the trigger pulse. This signal places the S/H into the Hold mode and starts the timing logic. At this time, the internal logic locks out any additional triggers that may inadvertently occur and corrupt the conversion process until the routine is complete. The path of the 10V p-p input signal during the first pass is through a 5:1 attenuator circuit to the 9-bit ADC with an input range of 2V p-p. At 50 ns, the ADC converts the signal and the 9 bits are latched both into the logic as the MSBs and into the 16-bit accurate DAC for the second pass.

The second pass subtracts the 9-bit, 16-bit accurate DAC output and the S/H output with the result equal to the 9-bit quantization error of the DAC, or 19.5 mV p-p. This "error" voltage is then amplified by a gain of 25.6 and is now 0.5V p-p or 1/4 of the full scale range of the ADC allowing a 2-bit overlap safety margin. At approximately 1.2 µs, the DAC and the "error" amplifier have had sufficient time to settle to 16-bit accuracy and the amplified "error" voltage is then digitized by the ADC with the 9-bit second pass result latched into the logic. At this time the S/H returns to the Sample mode to begin acquiring the next sample.

The 1/4 full scale range in the second pass produces a 2-bit overlap of the two passes. This is a scheme used in the A/D converter to provide an output word that is accurate and linear to 16 bits. This method corrects for any gain and linearity errors in the amplifying circuitry, as well as the 9-bit flash A/D converter. Without the use of this overlapping correction scheme, it would be necessary that all the components in the A/D converter be accurate to the 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it clearly would be impractical to achieve on a production basis. The key to the conversion technique used in the A/D converter is the 16-bit accurate and 16-bit-linear D/A converter which serves as the reference element for the conversion's second pass. The use of proprietary sub-ranging architecture in the A/D converter results in a sampling A/D converter that offers unprecedented speed and transfer characteristics at the 16-bit level.

The ADC4345 has a 3-state output structure. Users can enable the eight MSBs and B1 with $\overline{\text{HIBYTEN}}$ and the eight LSBs with $\overline{\text{LOBYTEN}}$ (both are active low). This feature makes it possible to transfer data from the A/D converter to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered (see Figure 7).

Figure 7 shows a typical application circuit for the A/D converter: a four channel, high speed, high resolution A/D conversion system tied into an 8-bit bus structure. This circuit could be part of the front end of a medical imaging system, an ATE system or a sampling oscilloscope. The 16-bit resolution provides 96 dB dynamic range for each channel, and the 500 kHz throughput rate provides approximately 125 kHz throughput per channel. (In certain CT imaging applications, it may be possible to multiplex as many as 24 channels into the A/D converter.)

For multiplexed inputs, the high input impedance of the on board buffer input is required. By addressing the multiplexer at the time of the ADC trigger (Figure 5), the mux and buffer settling times do not add to the system throughput rates.

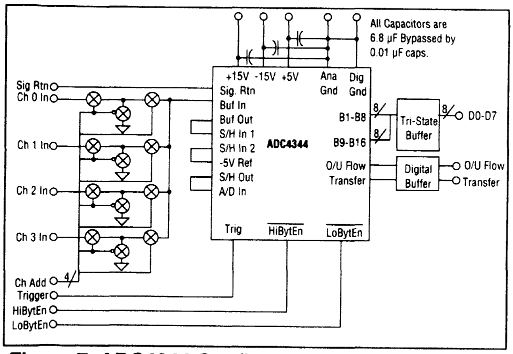


Figure 7. ADC4344 Configured for: 4-CH input, 0V to +10V input range, true binary data driving an 8-bit bus.

For interfacing into a 16-bit bus, the tri-state latch or digital buffers may still be required to prevent coupling of high frequency noise from the microprocessor bus into the A/D converter. Note that in Figure 7 the signal return is NOT tied to the external common ground-plane return but instead is common at a strategic point inside the A/D converter.

Both the ability of the A/D converter Sample-and-Hold amplifier to acquire new data to within ±1 LSB after a full-scale step change at the analog input, and the superb dc characteristics exhibited by the A/D converter, are key factors in establishing this part as the ideal choice for high speed, high performance data acquisition systems.

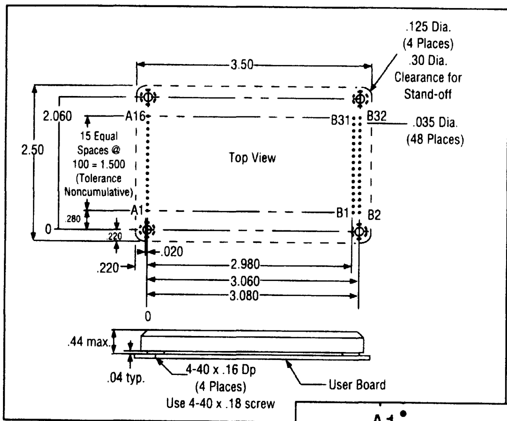
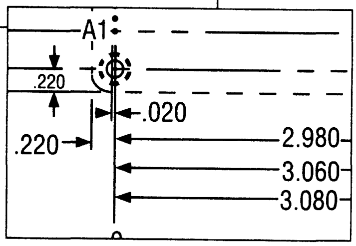


Figure 8. ADC4344/ ADC4345 Mechanical.



A1	+15V	B1	+5V	B2	+5V
A2	AGND	B3	DGND	B4	DGND
A3	–15V	B5	N.C.	B6	N.C.
A4	BUFFER IN	B7	N.C.	B8	N.C.
A5	BUFFER OUT	B9	N.C.	B10	N.C.
A6	A/D IN	B11	BIT1	B12	BIT1
A7	S&H OUT	B13	BIT2	B14	BIT3
A8	S&H IN1	B15	BIT4	B16	BIT5
A9	S&H IN2	B17	BIT6	B18	BIT7
A10	SIG RTN	B19	BIT8	B20	BIT9
A11	SIG RTN	B21	BIT10	B22	BIT11
A12	SIG RTN	B23	BIT12	B24	BIT13
A13	+5V REF	B25	BIT14	B26	BIT15
A14	OFF-SET ADJ	B27	BIT16	B28	TRIGGER
A15	GAIN ADJ	B29	TRANSFER	B30	$\overline{\text{LOBYTE ENB}}$
A16	–5V REF	B31	$\overline{\text{HIBYTE ENB}}$	B32	O/U FLOW

Figure 9. ADC4345 Pin Assignment.

Ordering Guide

Simply Specify
ADC4344M – 1 MHz
ADC4345M – 500 kHz

ADC4355/ADC4356/ ADC4357

Low Noise, Low Distortion, High Speed, 16-Bit Sampling A/D Converters

Designed for High Performance Applications

Introduction

The Analogic ADC435X series of products consists of high speed, low noise, low distortion, 16-bit A/D converters. The ADC4355 and ADC4357 are sampling A/D converters that have throughput rates of 100 kHz and 200 kHz respectively; the ADC4356 is a 7 µs buffered A/D converter. Designed for high performance applications, they are pin-compatible to the industry standard Analogic MP2735A and AM40516 A/D converters. The ADC435X converters are ideally suited for applications where high speed, true 16-bit linearity, and excellent frequency domain features are a must, such as spectroscopy, professional digital audio, telecommunications, ATE, and medical imaging.

The ADC435X series features excellent differential nonlinearity of ±1/2 LSB, a low 35 µV rms noise, and optional bipolar or unipolar 10V input ranges. The ADC435X series utilizes a 3-pass subranging architecture that both minimizes parts count and yields unprecedented stability, linearity, and accuracy. To achieve its superior performance, the ADC435X relies on a proprietary reference D/A converter that has inherent 16-bit accuracy and linearity. Use of a CMOS flash A/D converter eliminates the −5V requirement, an inconvenience in most high speed 16-bit ADCs. With TTL and CMOS-compatibility, tri-state data outputs, self-contained reference and timing circuitry, the ADC435X series offers easy system integration conveniently packaged in a 3" x 4" fully shielded module.

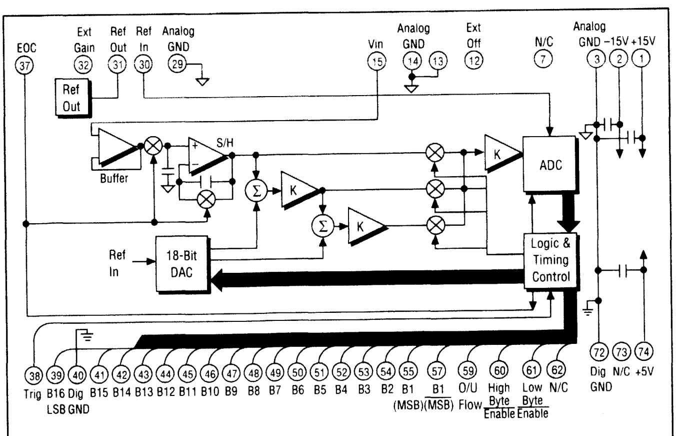
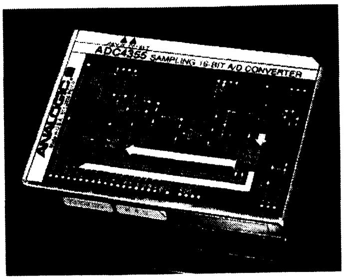


Figure 1. ADC4355/ADC4356/ADC4357 Functional Block Diagram and Pinout.



Features

- ❑ 16-Bit Resolution
- ❑ No Missing Codes
- ❑ Wide Dynamic Range: 96 dB
- ❑ Signal to Noise Ratio: 95 dB
- ❑ Peak Distortion: −110 dB (1 kHz)
- ❑ Total Harmonic Distortion: −103 dB (1 kHz)
- ❑ ±0.5 LSB Differential Non-Linearity
- ❑ 200 kHz Throughput Rate (ADC4357)
- ❑ 100 kHz Throughput Rate (ADC4355)
- ❑ Ease of Use
- ❑ Built-In S/H Amplifier (ADC4355/57)
- ❑ TTL Compatibility
- ❑ No −5V Requirement
- ❑ High Input Impedance
- ❑ Electromagnetic/Electrostatic Shielding

Applications

- ❑ Professional Audio Encoding
- ❑ Digital Telecommunications
- ❑ Automatic Test Equipment
- ❑ High-Resolution Imaging
- ❑ Spectroscopy
- ❑ Medical Data Acquisition
- ❑ Satellite Communications
- ❑ Multiplexed Data Acquisition

	ADC4355/ADC4356			ADC4357			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
ANALOG INPUT							
Input Range (2)							
Unipolar	0		+10	0		+10	V
Bipolar	-5		+5	-5		+5	V
Input Bias Current		0.5 µA	2 µA		1 nA	50 nA	
Input Capacitance		10			10		pF
Input Resistance	100			100			MΩ
Max. Input without Damage		±Supplies			±Supplies		
DIGITAL INPUTS							
Logic Levels	LSTTL/CMOS-Compatible			LSTTL/CMOS-Compatible			
Logic "0"			0.8			0.8	V
Logic "1"	2.0			2.0			V
Trigger	Positive Edge Triggered			Positive Edge Triggered			
Loading			1			1	LSTTL
Pulse Width	50			50			ns
High Byte Enable	Active Low, B1-B8, $\overline{B1}$			Active Low, B1-B8, $\overline{B1}$			
Low Byte Enable	Active Low, B9-B16			Active Low, B9-B16			
Propagation Delay with 1 TTL Load		20	50		20	50	ns
DIGITAL OUTPUTS							
Logic Levels							
Logic "0"			+0.4			+0.4	V
Logic "1"	+2.4			+2.4			V
Fan-Out			1			0.1	TTL Load
Output Coding	Binary Offset, Binary, Two's Complement, Complementary Data (see ordering guide)			Binary Offset, Binary, Two's Complement Complementary Data (see ordering guide)			
End of Conversion (EOC)	High during conversion, data valid 10 ns min. prior to falling edge			High during conversion, data valid 10 ns min. prior to falling edge			
Over/Under Flow	Active high at ±FS, not tri-stateable			Active high at ±FS, not tri-stateable			
REFERENCE							
Voltage Output		-6.5			–6.5		V
Load (3)			1			1	mA
Input Loading							
±5V Input	720Ω // 10 µF, -1.5 mA typ.			720Ω // 10 µF, -1.5 mA typ.			
0V to +10V Input	607Ω // 10 µF, -3.5 mA typ.			607Ω // 10 µF, -3.5 mA typ.			
Max Input W/O Damage	+0.5		-8.5	+0.5		-8.5	V
DYNAMIC CHARACTERISTICS							
Maximum Throughput Rate	100			200			kHz
A/D Conversion Time	7				4		µs
S/H Acquisition Time		3			1		µs
S/H Aperture Delay		30	60		30	60	ns
S/H Aper. Jitter		200	400		100	200	ps RMS
S/H Feedthrough (4)		-96	-90		-96	-90	dB
Sig. to Noise Ratio (5)	92	95		86	90		dB
Peak Distortion (6)							
±5V Input @ 1 kHz		-110	-100				dB
±5V Input @ 10 kHz					-100	-95	dB
±5V Input @ 20 kHz		-105	-96				dB
±5V Input @ 80 kHz					-90		dB
Total Harm. Dist. (7)							
±5V Input @ 1 kHz		-103	-94				dB
±5V Input @ 10 kHz					-94	-88	dB
±5V Input @ 20 kHz		-100	-94				dB
±5V Input @ 80 kHz					-87		dB

	ADC4355/ADC4356 Min.	Typ.	Max.	ADC4357 Min.	Typ.	Max.	Units
TRANSFER CHARACTERISTICS							
Resolution	16			16			Bits
Quantization Error			±0.5			±0.5	LSB
Int. Nonlinearity			±0.003			±0.003	% FSR
Diff. Nonlinearity		±0.25	±0.5		±0.5	±0.75	LSB
No Missing Codes	Guaranteed from 0°C to 60°C			Guaranteed from 0°C to 60°C			
Offset Error (8)			±1			±1	mV
Gain Error (8)			±0.01			±0.01	% FSR
Noise							
ADC4355		35					μV rms
ADC4356		25					μV rms
ADC4357					60		μV rms
External Offset Adjust		7.6			7.6		mV/V
External Gain Adjust		3.3			3.3		mV/V
STABILITY (0°C TO 60°C)							
Differential Nonlinearity			±0.5			±0.5	ppm /°C
Offset Voltage			±10			±10	ppm FSR/°C
Gain			±10			±10	ppm FSR/°C
Warm-Up Time			5			5	Mins.
Supply Rejection							
Offset		±5	±10		±5	±10	ppm FSR/%
Gain		±5	±10		±5	±10	ppm FSR/%
POWER REQUIREMENTS (10)							
±15V Supplies (9)	±11.65		±15.45	±11.65		±15.45	V
+5V Supply	+4.75		+5.25	+4.75		+5.25	V
±15V Current Drain							
ADC4355		58					mA
ADC4356		51					mA
ADC4357					62		mA
+5V Current Drain		55			55		mA
Power Consumption							
ADC4355		2.0					W
ADC4356		1.8					W
ADC4357					2.2		W
ENVIRONMENTAL & MECHANICAL							
Temperature Range							
Rated Performance	0		60	0		60	°C
Storage	-25		80	-25		80	°C
Relative Humidity							
Non-condensing	0 to 85 % up to 60°C			0 to 85 % up to 60°C			
	Dimensions 3" x 4" x 0.44" (76.2 x 127 x 11.18 mm)			Dimensions 3" x 4" x 0.44" (76.2 x 127 x 11.18 mm)			
Shielding	Electromagnetic 5 Sides, Electrostatic 6 Sides			Electromagnetic 5 Sides, Electrostatic 6 Sides			
Case Potential	Ground			Ground			

NOTES:

1. Unless otherwise noted, all specifications apply at 25°C and power supplies are ±15V and +5V.
2. See ordering guide for factory-set input ranges.
3. Reference load must remain constant during conversion. DC load 1mA max.
4. Measured with a 20 kHz full scale sine wave input.
5. Signal-to-Noise Ratio represents the ratio between the rms value of the signal and the total rms noise below the Nyquist Rate. The total rms noise is computed by: (l) summing the noise power in all frequency bins not correlated with the test signal; (2) estimating the total noise power contained in all harmonically related frequency bins; and (3) computing the rms noise from the sum of (l) and (2).
6. Peak Distortion represents the ratio between the highest spurious frequency component below the Nyquist rate and the signal. Note that in computing Peak Distortion, the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 5.
7. Total Harmonic Distortion represents the ratio between the rms sum of all harmonics up to the 100th harmonic and the rms value of the signal. Note that in computing THD, the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 5.
8. Externally adjustable to zero.
9. For the 0V to +10V input voltage range, the minimum analog supply voltage is ±14.55V.
10. Analogic highly recommends the use of linear power supplies with its high performance, high resolution A/D converters. However, if system requirements provide only a +5V supply and limited space, the use of the Analogic SP7015 DC-to-DC converter will provide a low noise solution which will not degrade the ADC4355/ADC4356/ADC4357 performance.

Specifications subject to change without notice.

SPECIFICATIONS

Output Coding and Trim Procedure

Figure 2 shows the output coding of the ADC435X A/D converter. The symbol * in Figure 2 indicates a bit that is undergoing a 0/1 or 1/0 code transition at the indicated analog input voltage.

To trim the offset of the ADC435X, apply 76 μV to the analog input. Adjust the offset trim potentiometer such that the digital output corresponds to the truth table of Figure 2.

To trim the gain of the ADC435X apply +4.999924V for the bipolar option or +9.999772V for the unipolar option. Adjust the gain trim potentiometer such that the digital output corresponds to the truth table of Figure 2.

In addition to the internal offset and gain potentiometers, provisions have been made to externally null out DC errors by use of potentiometers or DACs. A 10V swing from a DAC on Pin 12 produces a 33 mV offset shift; a 10V swing on Pin 32 produces a 76 mV gain shift.

TRUTH TABLE

INPUT VOLTAGE	DIGITAL OUTPUTS	
	COMP. OFFSET BINARY	STRAIGHT OFFSET BINARY
	MSB LSB	MSB LSB
BIPOLAR		
5.000000V	0000000000000000	OVERFLOW
4.999924V	000000000000000*	OVERFLOW
4.999848V	0000000000000001	1111111111111111
+0.000152V	0111111111111111	1000000000000001
+0.000076V	****************	100000000000000*
0.000000V	1000000000000000	1000000000000000
-4.999695V	1111111111111110	0000000000000010
-4.999771V	111111111111111*	00000000000000**
-4.999848V	1111111111111111	0000000000000001
-5.000000V	OVERFLOW	0000000000000000
UNIPOLAR		
9.999848V	0000000000000000	1111111111111111
9.999772V	000000000000000*	111111111111111*
9.999695V	0000000000000001	1111111111111110
5.000000V	0111111111111111	1000000000000000
4.999924V	****************	****************
4.999848V	1000000000000000	0111111111111111
0.000152V	1111111111111110	0000000000000001
0.000076V	111111111111111*	000000000000000*
0.000000V	1111111111111111	0000000000000000

Figure 2. Output coding for the ADC435X.

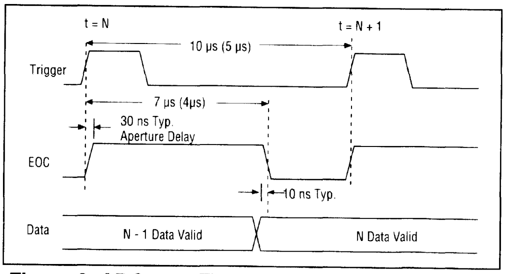


Figure 3. ADC435X Timing Diagram.

Timing Considerations

The timing diagram of Figure 3 shows the timing characteristics of the ADC435X A/D converter. Numbers in parentheses are figures for the ADC4357. Upon a low-to-high transition of the trigger input, the end of conversion (EOC) line also switches high. The EOC line in turn switches the internal sample-and-hold amplifier to the Hold mode; the S/H amplifier remains in the Hold mode for the duration of the A/D conversion period. At the end of the 7 μs (4 μs) A/D conversion period, the EOC line goes low and switches the sample-and-hold amplifier to the Sample mode. At the 100 kHz (200 kHz) throughput rate shown in Figure 3, the sample-and-hold amplifier then has 3 μs (1 μs) to sample (acquire) a new signal level for the next conversion cycle. The TTL-level Trigger input should have a minimum pulse width of 50 ns. Note that the data for a given conversion cycle becomes valid approximately 10 ns prior to the high-to-low transition of the EOC line.

Layout Considerations

Because of the extremely high resolution of the ADC435X A/D converter, it is necessary to pay careful attention to the printed circuit layout for the device. It is, for example, important to separate the analog and digital grounds and to return them separately to the system power supply. Digital grounds are often noisy or "glitchy", and these glitches can have adverse effects on the performance of a 16-bit A/D converter if they are introduced to the analog portions of the A/D converter's circuitry. At 16-bit resolution the size of the voltage step between one code transition and the succeeding one is only 153 μV, so it is evident that any noise in the analog ground return can result in erroneous or missing codes. It is therefore important to configure a low-impedance ground-plane return on the printed circuit board. Note that the ground-potential metal case used for the ADC435X provides shielding against electromagnetic interference on five sides and against electrostatic interference on six sides.

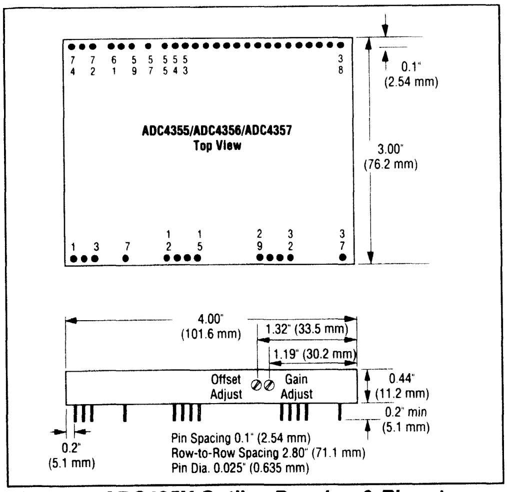


Figure 4. ADC435X Outline Drawing & Pinouts.

Principles of Operation

To understand the operating principles of the ADC435X A/D converter, refer to Figure 5. The simplified block diagrams in Paths a, b, and c in Figure 5 illustrate the three successive passes in the sub-ranging conversion scheme of the ADC435X. For all three passes, the lines labeled "From Input" come either from the output of the sample-and-hold amplifier (in the ADC4355/ADC4357) or from the output of the input buffer amplifier (in the ADC4356). In the first pass (a), a switched-gain amplifier attenuates the input signal by a factor of five. It thus converts the 10V full-scale range of the input to the 2V full-scale range of the 6-bit flash A/D converter. The 6-bit A/D converter then digitizes the six MSBs of the input signal. The outputs of the A/D converter drive the six MSBs of the D/A converter. Although not shown (for reasons of clarity) in Figure 5, the six output lines of the A/D converter are actually latched into the logic circuitry of a specialized gate array that drives the input lines of the D/A converter.

In the second pass (b), a difference amplifier subtracts the D/A converter's output voltage from the input voltage, then amplifies this difference by a factor of 3.2. The switched-gain amplifier now has a gain of two, and thus amplifies the difference voltage further. The output of the switched-gain amplifier again provides the input signal for the 6-bit flash A/D converter. The A/D converter's outputs are latched into the gate array that supplies the next lower-order bits of the D/A converter. In the gate array, the A/D converter's MSB in the second pass "overlaps" the LSB from the first pass. The resolution of the A/D conversion in the second pass is thus 11 bits (not 12) .

In the third pass (c), the gain of 3.2 difference amplifier subtracts the D/A converter's output voltage from the input voltage. In this pass, an amplifier with a gain of 32 provides additional amplification of the difference signal. The six outputs of the 6-bit flash A/D converter are latched into the gate array; the MSB of this conversion cycle "overlaps" the LSB of the previous cycle. The effective resolution of the conversion is thus 5 + 5 + 6, or 16 bits. Using the "overlap" structure, logic circuitry in the gate array adds the digital words produced in the three passes and produces the corrected output word. This digital error-correction technique thus provides an output word that is accurate and linear to within the full resolution of the A/D converter. The

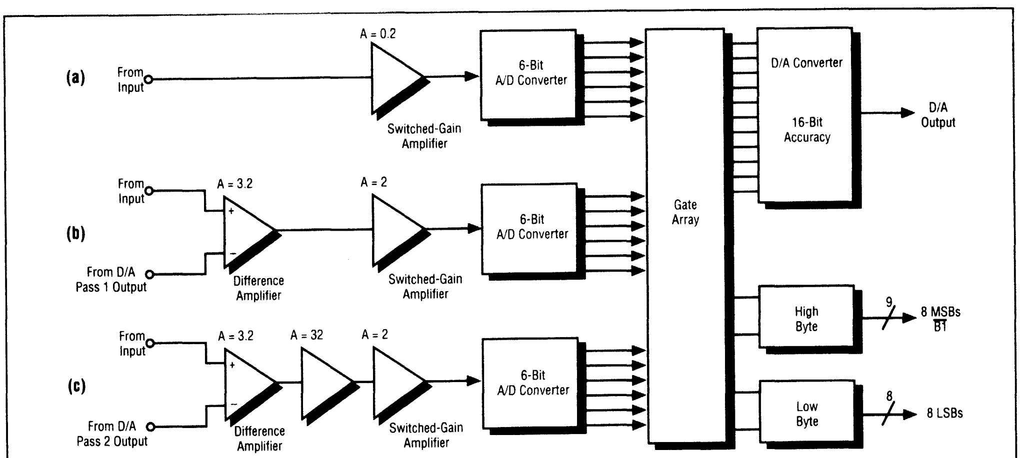


Figure 5. Operating Principle of the ADC435X.

method helps to compensate for any gain and linearity errors in the amplifying circuitry as well as in the 6-bit flash A/D converter. Without the error-correction technique, it would be necessary that all the components in the ADC435X — the difference amplifier, the switched-gain amplifier, and the 6-bit flash A/D converter — be accurate and linear to a 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it clearly would be impractical to achieve in production. The key to the ADC435X's conversion scheme is the 16-bit-linear D/A converter, which serves as a reference element for the conversion passes as well as for the error-correction mechanism.

The ADC435X has a tri-state output structure. Users can enable the eight MSBs, eight LSBs, or both by using the High-Byte Enable and Low-Byte Enable pins (both pins are active low). This feature makes it possible to transfer data from the ADC435X to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered (see Figure 6).

Typical Application

Figure 6 shows a typical application circuit for the ADC4356 16-bit A/D converter. This circuit provides simultaneous sampling of eight bipolar analog-input channels. Simultaneous sampling is a necessity in conversion systems in which the phase, as well as amplitude, relationship between different signals is an important parameter. One example is in seismic measurements, in which it is crucial to know the phase relationship between the signals generated by different sensors. This application circuit performs simultaneous sampling by "freezing" the signal levels of eight analog-input channels at the same instant of time. The differential multiplexer then presents these signal levels, either sequentially or in any user-programmed order, to the ADC4356 A/D converter via a differential amplifier. Although the input signals to this circuit are essentially single-ended, the use of a differential multiplexer and a differential amplifier eliminates the possibility of errors arising from common mode voltages.

The minicomputer or microprocessor in Figure 6 provides the sequence and timing information to the control logic. The control logic then performs the task of switching the sample-and-hold amplifiers from Sample to Hold mode and vice-versa, selecting the appropriate input channel and triggering the ADC4356 A/D converter. By using two resistors with each SHA2410 sample-and-hold amplifier, a user can program the SHA2410s to provide the gain required to match the input signals to the ±5V full-scale range of the ADC4356 A/D converter. In the application circuit of Figure 6, for example, the four inputs shown have full-scale ranges of ±1, ±2, ±3, and ±5V. The eighth input channel has the proper full-scale range of ±5V, so gain-setting resistors are not required. Because the SHA2410s provide the sample-and-hold function in this circuit, the ADC4356, which does not include a sample-and-hold amplifier, is an appropriate choice.

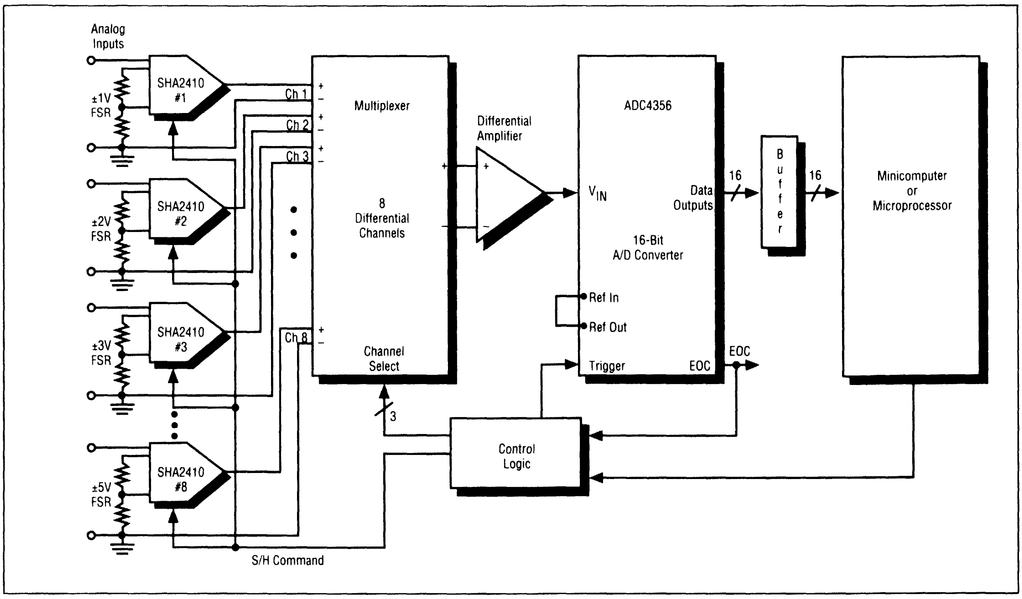


Figure 6. Typical Application Circuit for the ADC4356.

Ordering Guide

ADC435_ -M _ _

5	100 kHz Sampling
6	7 µs Buffered A/D Converter
7	200 kHz Sampling ADC
1	0V to +10V Input
4	±5V Input
S	Straight Data
C	Complementary Data

DC-to-DC Converter **SP7015**

ADC3120

Very High Speed, Very High SFDR, 14-Bit, 20 MHz Sampling A/D Converter

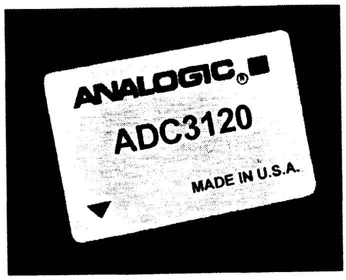
In a Space-saving 46-Pin Hybrid Package

Introduction

The ADC3120 is a complete 14-bit, 20 MHz A/D converter subsystem with a built-in sample-and-hold amplifier in a space-saving 46-pin hybrid package. It is designed for use in applications requiring high speed and high resolution front ends, such as ATE, digital oscilloscopes, medical imaging, radar, and digital receivers. The ADC3120 is capable of digitizing a 10 MHz signal at a 20 MHz sampling rate with a guarantee of no missing codes from 0°C to +70°C. Equally impressive in frequency domain applications, the ADC3120 features 75 dB signal-to-noise ratio with input signals from DC to 10 MHz and a spurious free dynamic range of 88 dB up to 10 MHz.

The ADC3120 utilizes the latest semiconductor technologies to produce a cost-effective, high performance part in a 46 pin hybrid package. It is designed around a pipelined sub-ranging architecture that integrates a pair of low-distortion, sample-and-hold amplifiers; a 3-bit, 14-bit accurate, flash/DAC; a high-speed, 12-bit sampling ADC, all necessary timing circuitry; and ECL-compatible output lines for ease of system integration.

Superior performance and ease of use make the ADC3120 the ideal solution for those applications requiring a sample-and-hold amplifier directly at the input to the A/D converter. Having the S/H amplifier integrated with the A/D converter benefits the system designer in two ways. First, the S/H is designed specifically to complement the performance of the A/D converter; for example, the acquisition time, hold mode settling and droop rate are optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves true 14-bit performance, avoiding degradation due to ground loops, signal coupling, jitter and digital noise introduced when separate S/H and A/D converters are interconnected. Furthermore, the accuracy, speed, and quality of the ADC3120 are fully ensured by thorough, computer factory tests of each unit.



Features

- ❑ Built-in S/H Amplifier
- ❑ 14-Bit Resolution
- ❑ 20 MHz Conversion Rate
- ❑ 0.006% Maximum Integral Nonlinearity
- ❑ No Missing Codes
- ❑ Spurious Free Dynamic Range: 90 dB
- ❑ Signal to Noise Ratio: 75 dB
- ❑ Total Harmonic Distortion: –85 dB
- ❑ ECL Compatibility
- ❑ Compact Size: 46-Pin Hybrid DIP

Applications

- ❑ Digital Signal Processing
- ❑ Sampling Oscilloscopes
- ❑ Automatic Test Equipment
- ❑ Analytical Instrumentation
- ❑ Medical Instrumentation
- ❑ CCD Detectors
- ❑ IR Imaging
- ❑ Radar
- ❑ Digital Receivers

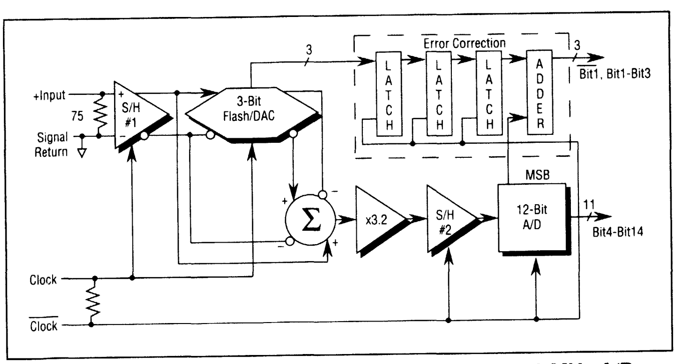


Figure 1. ADC3120 Functional Block Diagram, 14-bit 20 MHz A/D.

ANALOGIC®
The World Resource for Precision Signal Technology

ADC3120

Specifications[1]

ANALOG INPUT

Input Voltage Range
Bipolar
±1.280V

Maximum Input Without Damage
+5.25V
–5.45V

Input Resistance
75Ω

Input Capacitance
5 pF

CLOCK INPUTS

Compatibility
ECL

Logic "0"
–1.5V Max.

Logic "1"
–1.1V Min.

CLOCK
Positive Edge Puts S/H 1 into Hold

Duty Cycle
50% ±10%

CLOCK
Complementary CLOCK

Loading
100Ω Typ.

DIGITAL OUTPUTS

Fan-Out
Logic "0"
–1.5V Max.

Logic "1"
–1.1V Min.

Output Coding [2]
Offset binary, 2's Complement

DYNAMIC CHARACTERISTICS

Maximum Throughput Rate
20 MHz

Minimum Throughput Rate
10 MHz

S/H Aperture Delay
5 ns Max.

S/H Aperture Jitter
1 ps RMS Max.

Analog Bandwidth
80 MHz

Signal to Noise Ratio
DC to 10 MHz Input @ –1 dB
75 dB Min.

Spurious Free Dynamic Range
DC to 10 MHz Input @ –1 dB
90 dB Min.

Total Harmonic Distortion
1 MHz Input @ –1 dB
–85 dB Max.

10 MHz Input @ –1 dB
–82 dB Max.

Step Response
30 ns Max. to 0.01%

TRANSFER CHARACTERISTICS

Resolution
14 bits

Quantization Error
±0.5 LSB Max.

Integral Nonlinearity
±0.006% FSR Max.

Differential Nonlinearity
±0.75 LSB Max.

Monotonicity
Guaranteed

No Missing Codes
Guaranteed 0°C to +70°C

Noise
160 μV RMS Typ.

POWER REQUIREMENTS

±15V Supplies (±3%)
27 mA Typ.

–15V Supplies (±3%)
14 mA Typ.

+5V Supply (±5%)
285 mA Typ.

–5.2V Supply (±5%)
601 mA Typ.

Total Power Consumption
5.2W Typ.

ENVIRONMENTAL & MECHANICAL

Specified Temperature Range [3]
0°C to +70°C

Storage Temperature Range
–40°C to 125°C

Dimensions
1.6" x 2.4" x 0.225"
(40.64 mm x 60.96 mm x 5.714 mm)

Shielding
Electromagnetic 6 sides, Electrostatic 6 sides

Case Potential
Ground

Thermal Impedance
θ_{AC} = 10°C/W Typ.

Heat Sink Recommendations
Aluminum Block, 2.35" x 1" x 0.14"
(59.7 mm x 25.4 mm x 3.56 mm), or
Gap Pad on Ground Plane
(1.5 to 2 oz copper clad ground plane)

1. All specifications guaranteed at 50°C (Case) unless otherwise noted. Supplies at ±15V, and +5V.
2. For 2's Complement operation, simply use BIT 1 instead of BIT 1.
3. Specified temperature is guaranteed for case temperature.

Specifications subject to change without notice.

Principle Of Operation

The ADC3120 is a 14-bit sampling A/D converter that utilizes a two-pass, sub-ranging, pipelined architecture to achieve sampling rates from 10 MHz to 20 MHz. The analog input range is ±1.280V and is converted to an offset binary, or two's complement data format.

To understand the operating principles of the ADC3120, refer to the Functional Block Diagram of Figure 1 and Timing Diagram of Figure 2. Analog input signals up to 10 MHz are captured by a low-noise, low-distortion, S/H amplifier, S/H #1. S/H #1 drives both a three-bit flash DAC (14-bit linear) and the summing junction of a residue amplifier. The three MSBs of the flash/DAC are latched into the first of three registers within the error correction logic. The flash DAC will produce an analog voltage equal to the analog input of the ADC3120 to within three bits of resolution or an error voltage equal to 320 mV P-P. (It is critical that the flash DAC be at least 14-bit linear, as any error source will add directly to the 3-bit quantization error at the summing junction.) The flash DAC analog output result is summed with the S/H #1 analog output at the summing junction input of the residue amplifier. This completes the first pass.

The second pass starts with the residue amplifier. It amplifies the error voltage by 3.2 (0.32 x 3.2 = 1.024 Vp-p) to use 11 bits of the 12-bit ADC. S/H #2 is put into hold and the ADC is then clocked. The eleven LSBs are latched into the output logic (after two additional clocks) and the MSB is latched into the error correction logic to be summed with the three MSBs of the first pass creating a one bit overlap. This overlap corrects for any gain and linearity errors in the amplifying circuit. This completes the second pass.

Within the 12-bit ADC, there exists a 2 clock pipelined delay before the N data is available. To compensate for this delay, the three MSBs from the flash DAC must be delayed by 3 clocks to be in phase with the second pass. This is accomplished with three data latches within the error correction logic followed by a 1/2 clock adder delay. Collectively, this creates a 3-1/2 clock pipelined delay from N clock to available N data (see Figure 2).

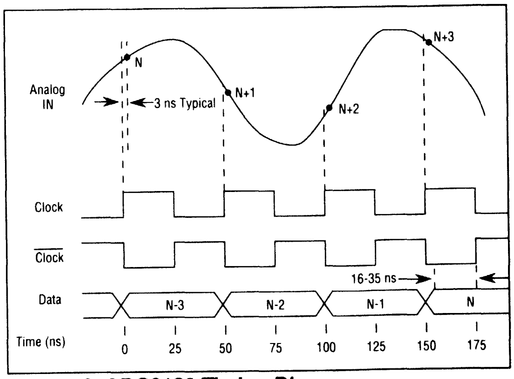


Figure 2. ADC3120 Timing Diagram.

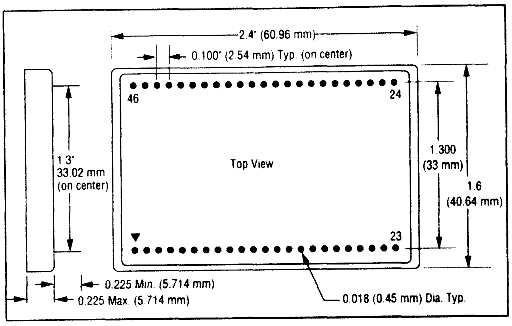


Figure 3. Outline Dimensions.

Interfacing

Pin #	Assignment	Pin #	Assigment
1	+5V	46	+5V
2	ANA RTN	45	−5.2V
3	SIG RTN	44	ANA RTN
4	SIG IN	43	ANA RTN
5	ANA RTN	42	ANA RTN
6	$\overline{\text{CLK}}$	41	ANA RTN
7	CLK	40	ANA RTN
8	−5.2V	39	ANA RTN
9	+5V	38	ANA RTN
10	N.C.	37	ANA RTN
11	ANA RTN	36	ANA RTN
12	−15V	35	ANA RTN
13	N.C.	34	+5V
14	+15V	33	ANA RTN
15	ANA RTN	32	−5.2V
16	ANA RTN	31	$\overline{\text{BIT 1}}$
17	BIT 14	30	BIT 1
18	BIT 13	29	BIT 2
19	BIT 12	28	BIT 3
20	BIT 11	27	BIT 4
21	BIT 10	26	BIT 5
22	BIT 9	25	BIT 6
23	BIT 8	24	BIT 7

Figure 3. ADC3120 Pin Assignment.

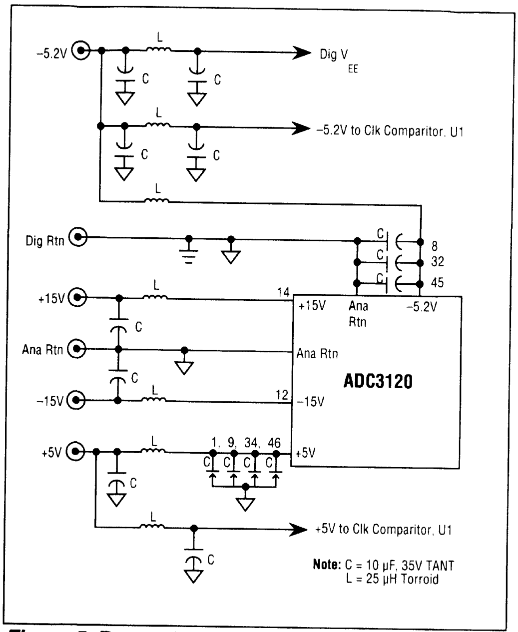


Figure 5. Bypassing the ADC3120.

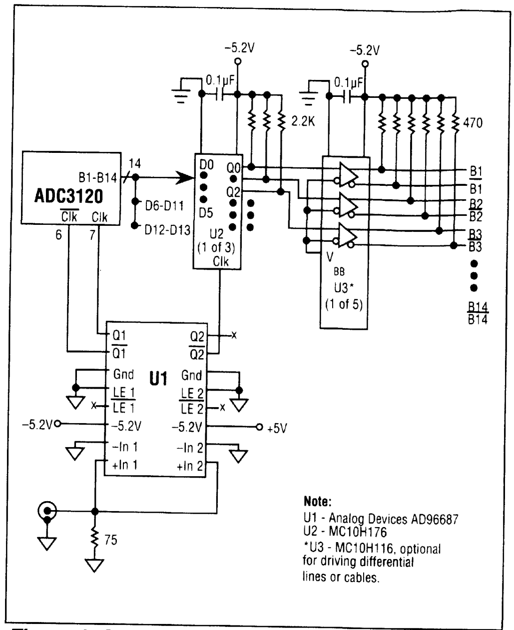


Figure 6. Suggested Clock and Data Interface Circuitry.

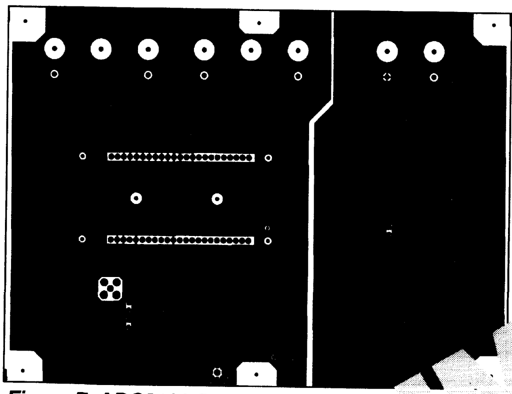


Figure 7. ADC3120-EB1 Primary Side Layout.

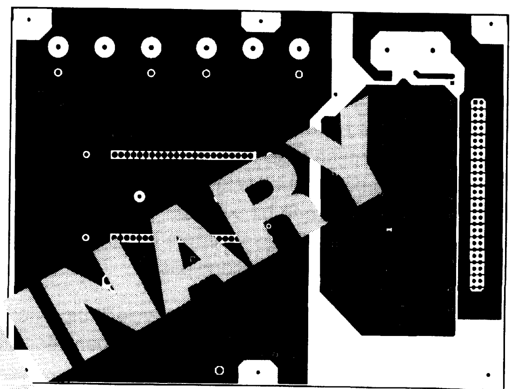


Figure 8. ADC3120-EB1 Secondary Side Layout.

ADC3121

Very High Speed 14-Bit, 20 MHz Sampling A/D Converter

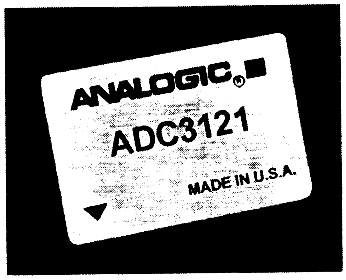
In a Space-saving 46-Pin Hybrid Package

Introduction

The ADC3121 is a complete 14-bit, 20 MHz A/D sampling A/D converter subsystem in a space-saving 46-pin hybrid package. It is designed for frequency domain applications requiring high speed and high resolution front ends, such as ATE, medical imaging, radar, I/Q Quadrature demodulators and digital receivers. With sampling rates of 10 MHz to 20 MHz, the ADC3121 is capable of 81 dB SFDR and 70 dB SNR. Sampling rates can easily be pushed to 20 MHz where performance specifications are 80 dB SFDR and 72 dB SNR. Although fully characterized in the frequency domain, the ADC3121 works equally well in applications requiring low noise and fast front end settling times, such as CCD detectors. The built-in sample-and-hold amplifier will settle to within one LSB in less than one conversion.

The ADC3121 utilizes the latest semiconductor technologies to produce a cost-effective, high performance part in a 46 pin hybrid package. It is designed around a pipelined sub-ranging architecture that integrates a pair of low-distortion, sample-and-hold amplifiers; a 3-bit, 14-bit accurate, flash/DAC; a high-speed, 12-bit sampling ADC; all necessary timing circuitry; and ECL-compatible output lines for ease of system integration.

The superior performance of the ADC3121 is due, in no small part, to the input sample-and-hold amplifier. It is a proprietary custom monolithic chip capable of settling to ±0.003% in just 25 ns! All the potential error sources were well defined and each was considered one at a time. The worst case analysis was performed and scrutinized closely. The result is a 10 MHz to 20 MHz sampling ADC with 81 dB SFDR and 72 dB SNR.



Features

- ❑ Built-in S/H Amplifier
- ❑ 14-Bit Resolution
- ❑ 10 MHz Sampling Rate
- ❑ 0.006% Integral Nonlinearity
- ❑ 81 dB SFDR
- ❑ 72 dB SNR
- ❑ ECL Compatibility
- ❑ Compact Size: 46-Pin Hybrid DIP

Applications

- ❑ Digital Signal Processing
- ❑ ATE
- ❑ Medical Imaging
- ❑ CCD Detectors
- ❑ IR Imaging
- ❑ Radar
- ❑ Digital Receivers
- ❑ I/Q Quadrature Demodulators

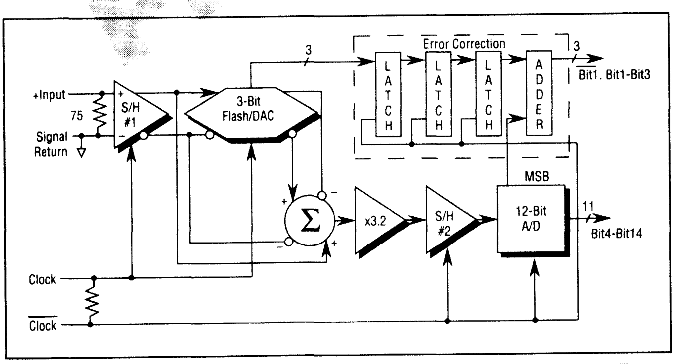


Figure 1. ADC3121 Functional Block Diagram, 14-bit 20 MHz A/D.

ADC3121

Specifications[1]

ANALOG INPUT

Input Voltage Range
Bipolar
±1.280V

Maximum Input Without Damage
+5.25V
–5.45V

Input Resistance
75Ω Typ.

Input Capacitance
5 pF Typ.

CLOCK INPUTS

Compatibility
ECL

Logic "0"
–1.5V Max.

Logic "1"
–1.1V Min.

Loading
100Ω Typ.

CLOCK (Complementary Inputs)
Positive Edge of CLOCK Puts S/H #1 into Hold

Duty Cycle
50% ±10%

DATA OUTPUTS

Fan-Out
1 ECL Load

Logic "0"
–1.5V Max.

Logic "1"
–1.1V Min.

Output Coding [2]
Offset binary, 2's Complement

TRANSFER CHARACTERISTICS

Resolution
14 bits

Integral Nonlinearity
±0.006% Max.

Differential Nonlinearity
±0.75 LSB Max.

Monotonicity
Guaranteed

No Missing Codes
Guaranteed over specified temperature range

Noise
160 µV RMS Typ.

DYNAMIC CHARACTERISTICS
(Minimum sampling rate is 10 MHz)

	(10 MHz Sampling)	*(20 MHz Sampling)*
S/H Aperture Delay	5 ns Max.	5 ns Max.
S/H Aperture Uncertainty	1 ps RMS Max.	1 ps RMS Max.
S/H Feedthrough	–90 dB Max.	–90 dB Max.
Full Power Bandwidth	80 MHz Max.	80 MHz Max.
Small Signal Bandwidth	80 MHz Min.	80 MHz Min.
Signal to Noise Ratio DC to 10 MHz Input @ –1 dB	70 dB Min.	72 dB Min.
Spurious Free Dynamic Range 2 MHz Input @ –0.5 dB	81 dB Min.	80 dB Min.
Spurious Free Dynamic Range 4.8 MHz Input @ –0.5 dB	81 dB Min.	73 dB Min.
Total Harmonic Distortion 2 MHz Input @ –0.5 dB	–78 dB Max.	–74 dB Max.
Total Harmonic Distortion 4.8 MHz Input @ –0.5 dB	–78 dB Max.	–70 dB Max.

POWER REQUIREMENTS

±15V Supplies (±3%)
27 mA Typ.

–15V Supplies (±3%)
14 mA Typ.

+5V Supply (±5%)
285 mA Typ.

–5.2V Supply (±5%)
601 mA Typ.

Total Power Consumption
5.2W Typ.

ENVIRONMENTAL & MECHANICAL

Specified Temperature Range [3]
0°C to +70°C

Storage Temperature Range
–40°C to 125°C

Ambient to Case ΔT (w/heat sink)
+37°C

Dimensions
1.6" x 2.4" x 0.225"
(40.64 mm x 60.96 mm x 5.715 mm)

Thermal Impedance
θ_{AC} = 10°C/W Typ.

Heat Sink Recommendations
Aluminum Block, 2.35" x 1" x 0.14"
(59.7 mm x 25.4 mm x 3.56 mm), or
Gap Pad on Ground Plane
(1.5 to 2 oz copper clad ground plane)

1. All specifications guaranteed at 50°C unless otherwise noted.
2. For 2's Complement operation, simply use $\overline{\text{BIT 1}}$ instead of BIT 1.
3. Specified temperature is guaranteed for case temperature.

Specifications subject to change without notice.

Principle Of Operation

The ADC3121 is a 14-bit sampling A/D converter that utilizes a two-pass, sub-ranging, pipelined architecture to achieve sampling rates from 10 MHz to 20 MHz. The analog input range is ±1.280V and is converted to an offset binary, or two's complement data format.

To understand the operating principles of the ADC3121, refer to the Functional Block Diagram of Figure 1 and Timing Diagram of Figure 2. Analog input signals up to 10 MHz are captured by a low-noise, low-distortion, S/H amplifier, S/H #1. S/H #1 drives both a three-bit flash DAC (14-bit linear) and the summing junction of a residue amplifier. The three MSBs of the flash/DAC are latched into the first of three registers within the error correction logic. The flash DAC will produce an analog voltage equal to the analog input of the ADC3121 to within three bits of resolution or an error voltage equal to 320 mV P-P. (It is critical that the flash DAC be at least 14-bit linear, as any error source will add directly to the 3-bit quantization error at the summing junction.) The flash DAC analog output result is summed with the S/H #1 analog output at the summing junction input of the residue amplifier. This completes the first pass.

The second pass starts with the residue amplifier. It amplifies the error voltage by 3.2 (0.32 x 3.2 = 1.024 Vp-p) to use 11 bits of the 12-bit ADC. S/H #2 is put into hold and the ADC is then clocked. The eleven LSBs are latched into the output logic (after two additional clocks) and the MSB is latched into the error correction logic to be summed with the three MSBs of the first pass creating a one bit overlap. This overlap corrects for any gain and linearity errors in the amplifying circuit. This completes the second pass.

Within the 12-bit ADC, there exists a 2 clock pipelined delay before the N data is available. To compensate for this delay, the three MSBs from the flash DAC must be delayed by 3 clocks to be in phase with the second pass. This is accomplished with three data latches within the error correction logic followed by a 1/2 clock adder delay. Collectively, this creates a 3-1/2 clock pipelined delay from N clock to available N data (see Figure 2).

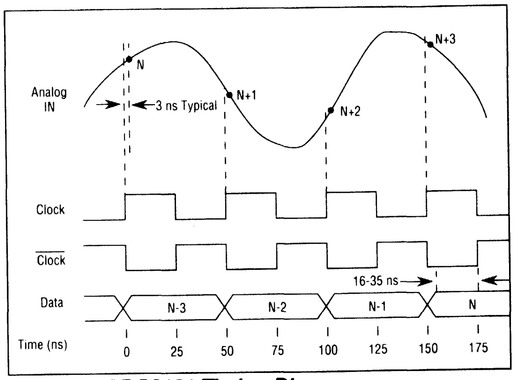


Figure 2. ADC3121 Timing Diagram.

Interfacing

Pin #	Assignment	Pin #	Assigment
1	+5V	46	+5V
2	ANA RTN	45	–5.2V
3	SIG RTN	44	ANA RTN
4	SIG IN	43	ANA RTN
5	ANA RTN	42	ANA RTN
6	$\overline{\text{CLK}}$	41	ANA RTN
7	CLK	40	ANA RTN
8	–5.2V	39	ANA RTN
9	+5V	38	ANA RTN
10	N.C.	37	ANA RTN
11	ANA RTN	36	ANA RTN
12	–15V	35	ANA RTN
13	N.C.	34	+5V
14	+15V	33	ANA RTN
15	ANA RTN	32	–5.2V
16	ANA RTN	31	$\overline{\text{BIT 1}}$
17	BIT 14	30	BIT 1
18	BIT 13	29	BIT 2
19	BIT 12	28	BIT 3
20	BIT 11	27	BIT 4
21	BIT 10	26	BIT 5
22	BIT 9	25	BIT 6
23	BIT 8	24	BIT 7

Figure 3. ADC3121 Pin Assignment.

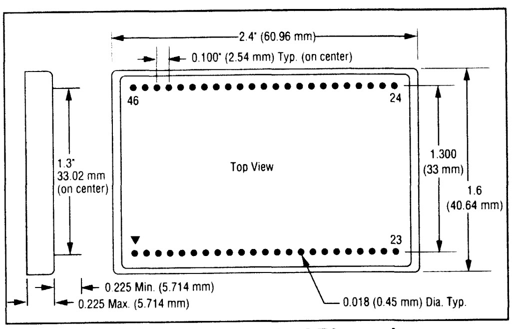


Figure 4. ADC3121 Mechanical Dimensions.

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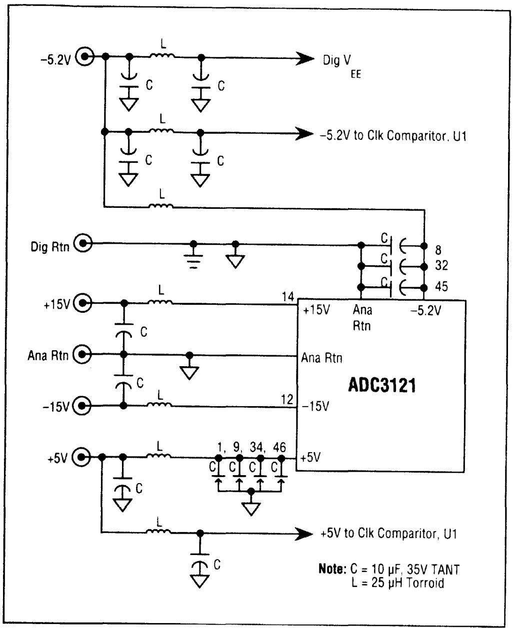


Figure 5. Bypassing the ADC3121.

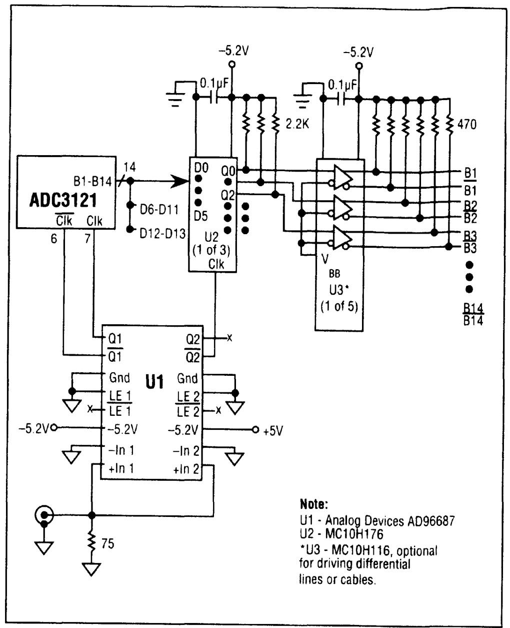


Figure 6. Suggested Clock and Data Interface Circuitry.

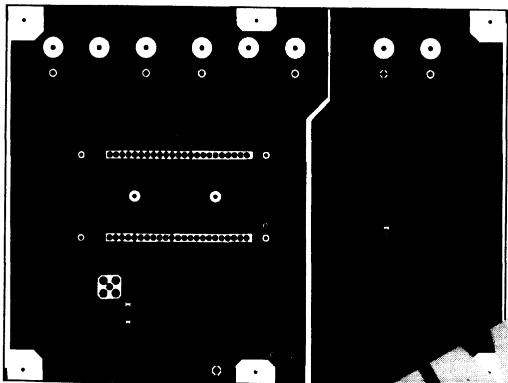


Figure 7. ADC3121-EB1 Primary Side Layout.

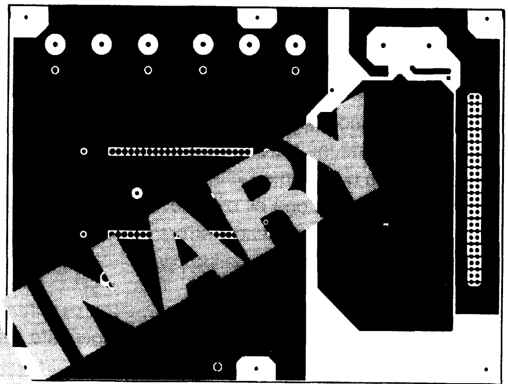
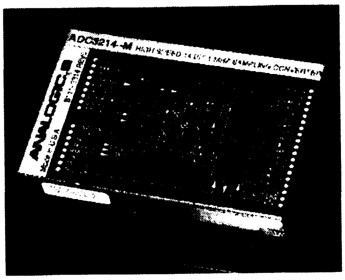


Figure 8. ADC3121-EB1 Secondary Side Layout.

ADC3214

High Speed, 14-Bit, 1 MHz, Sampling A/D Converter

With Built-in Sample-and-Hold Amplifier



Introduction

The ADC3214 is a 14-bit, 1 MHz A/D converter with a built-in sample-and-hold amplifier. It was designed for use in applications requiring high speed and high resolution front ends, such as ATE, medical imaging, radar, communications, and analytical instrumentation. The ADC3214 is a cost-effective solution for both time and frequency domain applications. It is capable of digitizing a 500 kHz signal at a 1 MHz rate with a guarantee of no missing codes. Signal-to-noise ratio is 76 dB at input frequencies from DC to 100 kHz. With a 1 MHz sampling rate and a full-scale step response to 14-bit accuracy of one conversion, this sampling A/D converter is ideally suited for applications with multiplexed signal sources.

The ADC3214 utilizes the latest surface-mount technologies to produce a cost-effective, high-performance part in a 2" x 3" fully shielded package. It is designed around a two-pass, subranging architecture that integrates a low distortion sample-and-hold amplifier, precision voltage reference, all the necessary timing circuitry and tri-state CMOS/TTL-compatible outputs for ease of system integration.

Continued on page 57.

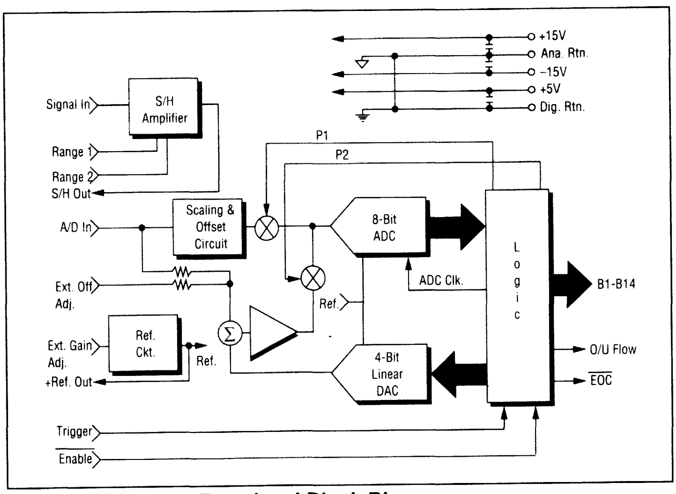


Figure 1. ADC3214 Functional Block Diagram.

Features

- ❑ 14-Bit Resolution
- ❑ 1 MHz Throughput Rate
- ❑ Reduced Cost
- ❑ Reduced Size
- ❑ No Missing Codes: 0°C to +60°C
- ❑ Signal-to-Noise Ratio: 76 dB
- ❑ Peak Distortion: –82 dB @ 100 kHz
- ❑ Total Harmonic Distortion: –80 dB @ 100 kHz
- ❑ Ease of Use
- ❑ Built-In S/H Amplifier
- ❑ TTL Compatibility
- ❑ High Input Impedance (100 MΩ)

Applications

- ❑ Radar
- ❑ Analytical Instrumentation
- ❑ Spectroscopy
- ❑ Digital Telecommunications
- ❑ Automatic Test Equipment
- ❑ High-Resolution Imaging
- ❑ Medical Data Acquisition
- ❑ Multiplexed Data Acquisition

ADC3214
Specifications[1]

ANALOG INPUT

Input Range
±1.25V, ±2.5V

Input Bias Current
5 nA Max.

S/H Input Capacitance
10 pF Typ.

S/H Input Resistance
100 MΩ Min.

A/D Input Resistance
1.25 kΩ to Ground

DIGITAL INPUTS

Compatibility
CMOS, TTL

Logic Levels
Logic "0"
–0.5V Min., 0.8V Max.

Logic "1"
2.0V Min., 5.5V Max.

Trigger
Negative Edge Triggered

Loading
1 TTL Load

Pulse Width
210 ns Min., 390 ns Max.

Output Enable
Active Low; B1-B14, O/U Flow

Propagation Delay
50 ns Max.

DIGITAL OUTPUTS

Maximum Output Drive
±2 mA Min.

Logic Levels
Logic "0"
0V Min., +0.4V Max.

Logic "1"
+3.5V Min., 5.0V Max.

Output Coding
Parallel Data, Offset Binary

EOC
Falling Edge, data valid 20 ns prior to falling edge

Over/Under Flow
Active High; 1/2 code below FS

INTERNAL REFERENCE

Voltage
10.0V Typ.

Stability
±15 ppm/°C Typ.

Available Current[2]
1 mA Max.

DYNAMIC CHARACTERISTICS

Maximum Throughput Rate
1 MHz Min.

A/D Conversion Time
600 ns Max.

S/H Aperture Delay
10 ns Typ.

S/H Aperture Jitter
15 ps RMS Typ., 30 ps RMS Max.

S/H Feedthrough[3]
–84 dB Typ., –80 dB Max.

Full Power Bandwidth
1.5 MHz Min., 2.5 MHz Typ.

Small Signal Bandwidth
3.5 MHz Typ.

Signal to Noise Ratio[4]
76 dB Min., 78 dB Typ.

Peak Distortion[5]
10 kHz
–86 dB Max., –95 dB Typ.

100 kHz
–82 dB Max., –89 dB Typ.

540 kHz
–76 dB Typ.

Total Harmonic Distortion[6]
10 kHz
–84 dB Max.

100 kHz
–80 dB Max.

540 kHz
–74 dB Typ.

Step Response[7]
400 ns to ±0.01%
500 ns to ±0.006%

TRANSFER CHARACTERISTICS

Resolution
14 bits

Quantization Error
±0.5 LSB

Relative Accuracy
±0.006% FSR Max.

Differential Non-Linearity
±0.75 LSB @ 25°C, ±1 LSB from 0°C to 60°C

Monotonicity
Guaranteed

No Missing Codes
Guaranteed from 0°C to 60°C

Offset Error[8]
±5 mV Max.

Gain Error[8]
±0.1% FSR Max.

Noise[9]
180 µV RMS Typ., 266 µV RMS Max.

STABILITY (0°C TO 60°C)

Differential Non-Linearity
±1 ppm FSR/°C Max.

Offset Voltage
±100 µV/°C Max.

Gain
±25 ppm FSR/°C Max.

Warm-Up Time
10 minutes

±15V Supply Rejection
±15 ppm FSR/% change Max.

Offset
±15 ppm FSR/% Change Max.

Gain
±15 ppm FSR/% Change Max.

+5V Supply Rejection
Offset
±60 ppm FSR/% Change Max.

Gain
±60 ppm FSR/% Change Max.

POWER REQUIREMENTS[10]

±15V Supplies
14.25V Min., 15.75V Max.

+5V Supply
+4.75V Min., +5.25V Max.

+15V Current Drain
48 mA Typ.

–15V Current Drain
63 mA Typ.

+5V Current Drain
132 mA Typ.

Power Consumption
2.35W Typ.

ENVIRONMENTAL & MECHANICAL

Temperature Range

Rated Performance
0°C to 60°C

Storage
–25°C to 75°C

Relative Humidity (Non-condensing)
0 to 85% to 60°C

Dimensions
1.99" x 2.99" x 0.44"
(50.5 x 75.9 x 11.2 mm)

Shielding
Electromagnetic 5 sides

Case Potential
Ground

NOTES

1. Unless otherwise noted, all specifications apply at 25°C ambient with power supplies of ±15V and ±5V.
2. External Reference Load to remain stable during conversion.
3. Measured with a full scale step input with a 20V/µs slew rate.
4. Signal-to-noise ratio represents the ratio between the RMS value of the signal and the total RMS noise below the Nyquist rate. The total RMS noise is computed by: (1) summing the noise power in all frequency bins not correlated with the test signal; (2) estimating the total noise power contained in all harmonic frequency bins; and (3) computing the RMS noise from the sum of (1) and (2).
5. Peak distortion represents the ratio between the highest spurious frequency component below the Nyquist rate and the signal. Note that in computing peak distortion the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 4.
6. Total harmonic distortion represents the ratio between the RMS sum of all harmonics up to the 100th harmonic and the RMS value of the signal. Note that in computing total harmonic distortion, the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 4.
7. Step Response represents the time required to achieve the specified accuracies after a full scale step change at the signal input, specified at a 1 MHz throughput rate.
8. Externally adjustable to zero. See coding and trim procedure.
9. Thermal noise from the S/H and A/D converter, not including quantization noise.
10. Analogic highly recommends the use of linear power supplies with its high performance, high resolution A/D converters. However, if system requirements provide only a +5V supply and limited space, the use of the Analogic SP7015 DC-to-DC converter will provide a low noise solution which will not degrade the ADC3214 performance.

Specifications subject to change without notice.

Continued from page 55.

Superior performance and ease-of-use make the ADC3214 the ideal solution for applications requiring a sample-and-hold amplifier directly at the input to the A/D converter. Having the S/H amplifier integrated with the A/D converter benefits the system designer in two ways. First, the S/H has been designed specifically to complement the performance of the A/D converter; for example, the acquisition time, hold mode settling and droop rate have been optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves true 14-bit performance, avoiding degradation due to ground loops, signal coupling, jitter and digital noise introduced when separate S/H and A/D convertesr are interconnected. Furthermore, the accuracy, speed, and quality of the ADC3214 are fully ensured by thorough, computer-controlled factory tests of each unit.

ADC3214 SPECIFICATIONS

Coding and Trim Procedure

Refer to Figures 2 and 3 for the ADC3214 Coding and Trim Procedure. Figure 2 shows the external Offset and Gain Adjust configuration. Figure 3 shows the output Offset Binary coding of the ADC3214 A/D converter. The voltages mentioned in the following Trim Procedure refer to the ±2.5V input range with the numbers in parentheses referring to the ±1.25V input range.

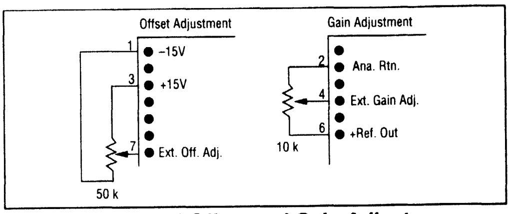


Figure 2. External Offset and Gain Adjust Configuration.

To trim the offset of the ADC3214, apply –153 µV (–76 µV) to the analog input. Adjust the external offset trim potentiometer such that each of the 14 bits alternates equally between "0" and "1". Using the setup as described in Figure 2, the sensitivity of the offset adjustment is typically 6 LSBs per volt.

To trim the gain of the ADC3214, apply +2.499542V (+1.249771V) to the analog input and adjust the external gain trim potentiometer such that the 13 MSBs are "1" and the LSB alternates equally between "0" and "1". Using the setup as described in Figure 2, the sensitivity of the gain adjustment is typically 0.14% per volt.

DIGITAL OUTPUT		ANALOG INPUT ±1.25V	±2.5V
MSB LSB			
1 1 1 1 1 1 1 1 1 1 1 1 1 1	=	+1.24985V	+2.49970V
1 0 0 0 0 0 0 0 0 0 0 0 0 0	=	0.00000V	0.00000V
0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	1.25000V	–2.50000V
B1,B2 . . . . .B14	=	Pin Label	

Figure 3. Output Coding for the ADC3214.

Timing Considerations

The timing diagram in Figure 4 shows the timing characteristics of the ADC3214 A/D converter. Upon a high-to-low transition of the Trigger input, the internal logic of the ADC3214 places the input S/H amplifier (see Figure 1) into the Hold mode. Approximately 550 ns after Trigger, the internal S/H amplifier returns to the Sample mode to begin acquiring the next sample.

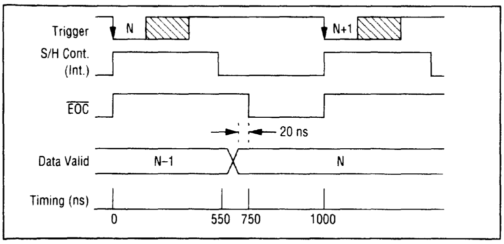


Figure 4. ADC3214 Timing Diagram.

Approximately 200 ns later (750 ns elapsed time), the A/D converter has completed the conversion process and latches the data into the output tri-state latches. The data is valid 20 ns prior to the high-to-low transition of the EOC pulse.

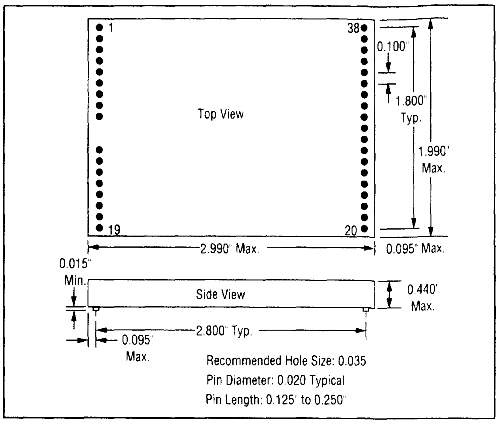


Figure 6. ADC3214 Mechanical.

Layout Considerations

The high resolution of the ADC3214 A/D converter makes it necessary to pay careful attention to the printed circuit layout for the device. It is, for example, important to separate analog and digital grounds and to return them separately to the system power supply. Digital grounds are often noisy or "glitchy," and these glitches can have adverse effects on the performance of the ADC3214 if they are introduced to the analog portions of the A/D converter's circuitry. At 14-bit resolution, the size of the voltage step between one code transition and the succeeding one is only 152 μV (305 μV for the ±2.5V range), so it is evident that any noise in the analog ground return can result in erroneous or missing codes. It is therefore important to configure a low-impedance ground-plane return on the printed-circuit board. This is the point where the analog and digital returns should be made common, NOT at the supplies.

1.	−15V	38.	DIG RTN
2.	ANA RTN	37.	+5V
3.	+15V	36.	O/U RANGE
4.	EXT RANGE ADJ	35.	BIT 1 (MSB)
5.	REF RTN	34.	BIT 2
6.	+V REF OUT	33.	BIT 3
7.	EXT OFFS ADJ	32.	BIT 4
8.	S/H ANA OUT	31.	BIT 5
9.	ADC IN	31.	BIT 6
10.	NO PIN	29.	BIT 7
11.	NO PIN	28.	BIT 8
12.	ANA RTN	27.	BIT 9
13.	SIGNAL IN	26.	BIT 10
14.	DO NOT CONNECT	25.	BIT 11
15.	RANGE 2	24.	BIT 12
16.	RANGE 1	23.	BIT 13
17.	DO NOT CONNECT	22.	BIT 14
18.	ANA RTN	21.	OUT ENABLE
19.	TRIGGER	20.	EOC

CONNECT PIN 8 TO PIN 9.

Figure 5. ADC3214 Pin Assignments.

PRINCIPLES OF OPERATION

To understand the operating principles of the ADC3214 A/D converter, refer to Figures 4 and 7. The simplified block diagram of Figure 7 illustrates the two successive passes in the sub-ranging conversion scheme of the ADC3214.

The ADC3214 is a 14-bit sampling A/D converter with throughput rates to 1 MHz. It has two externally configurable input ranges of ±1.25V and ±2.5V. This is easily accomplished by externally connecting Pins 15 and 16 for the ±1.25V range and leaving both pins open (N/C) for the ±2.5 range (see Figure 5). The S/H amplifier has a gain of X–1 or X–2, providing an output of ±2.5V regardless of the input. This simplifies the calibration of the ADC by reducing the required gain of the summing amplifier.

The first pass starts at a high-to-low transition of the trigger pulse. This signal places the S/H into the Hold mode and starts the timing logic. In the first pass, the output of the S/H is attenuated by a factor of 0.4 and offset to convert the 5V full scale ADC range to the 2V full scale range of the flash ADC. After approximately 110 ns, the attenuator circuitry has settled to 9-bit accuracy at which time the ADC digitizes the first pass. The 8 bits take two paths: to the internal logic and to the 8 most significant bits of a 14-bit accurate D/A converter, setting up the second pass.

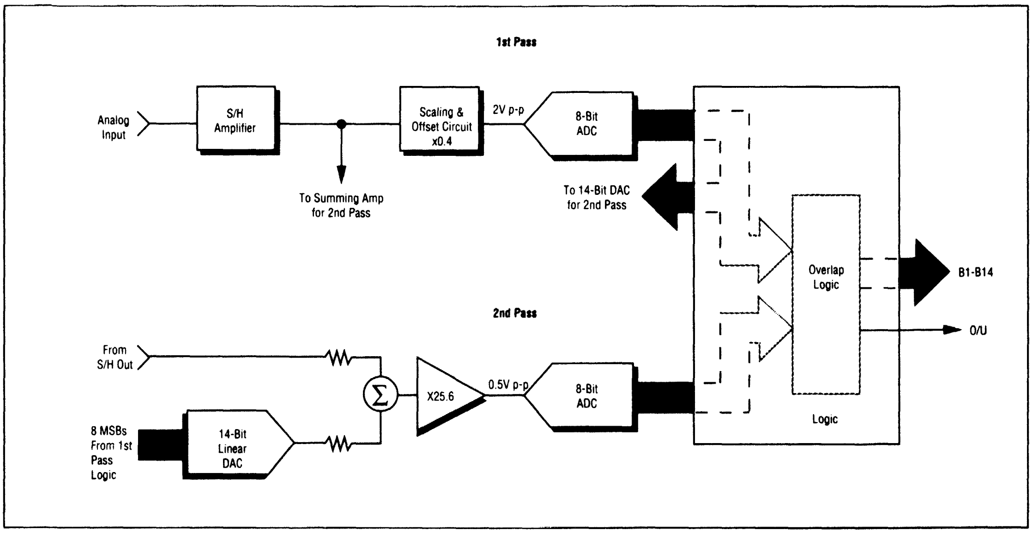


Figure 7. Simplified Block Diagram.

In the second pass, the output of the D/A converter is subtracted from the output of the S/H amplifier. The nominal error voltage of ±0.5 LSB (at the 8-bit level it is 5V/256 or 19.5 mV) is amplified by 25.6 to achieve 1/4 full scale range of the flash ADC, thus allowing a 2-bit overlap safety margin. The effective resolution therefore becomes the digital summation of two 8-bit results with the 2 LSBs of Pass 1 overlapping the 2 MSBs of Pass 2. At approximately 550 ns after trigger, the error signal has settled to 14-bit accuracy and the ADC then digitizes the second pass. The internal logic then places the S/H back into the Sample mode to begin acquiring the next sample. The second pass data is latched into the output tri-state registers and the conversion is now complete. This is marked by a high-to-low transition of the EOC pulse with the data valid 20 ns prior to EOC.

The ADC3214 has a tri-state output structure. Users can enable the fourteen data bits and the Overflow/Underflow bit with the ENABLE pin. This feature makes it possible to transfer data from the ADC3214 to a microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered (see Figure 8).

The 1/4 full scale range, or 2-bit overlap in the second pass, is a scheme used in the ADC3214 to provide an output word that is accurate and linear to 14 bits. This method corrects for gain and linearity errors in the amplifying circuitry, as well as the 8-bit flash A/D converter. Without the use of this overlapping correction scheme, it would be necessary that all the components in the ADC3214 be accurate to the 14-bit level. While such a design might be possible to realize on a laboratory benchtop, it clearly would be impractical to achieve on a production basis. The key to the conversion technique used in the ADC3214 is the 14-bit accurate and 14-bit linear D/A converter, which serves as the reference element for the conversion's second pass. The use of proprietary sub-ranging architecture in the ADC3214 results in a sampling A/D converter that offers unprecedented speed and transfer characteristics at the 14-bit level.

TYPICAL APPLICATION

Figure 8 shows a typical application circuit for the ADC3214-M A/D converter: an eight channel, high resolution, high speed data acquisition system. This circuit could be part of an automatic test system or the front end of a data acquisition and control system. The 14-bit resolution of the ADC3214 provides 84 dB dynamic range for each channel, and the 1 MHz throughput rate provides approximately 125 kHz throughput per channel.

For interfacing with a microprocessor-driven 16-bit bus, the use of digital buffers may be required to prevent coupling of high frequency noise from the microprocessor bus into the A/D converter. Note that in Figure 8, the signal return is NOT tied to the ground-plane return but instead is common at a strategic point inside the ADC3214.

The ability of the ADC3214 Sample-and-Hold amplifier to acquire new data to within ±1 LSB after a full-scale step change at the analog input and the superb DC characteristics exhibited by the ADC3214 are the key factors in establishing this part as the ideal choice for high speed data acquisition systems.

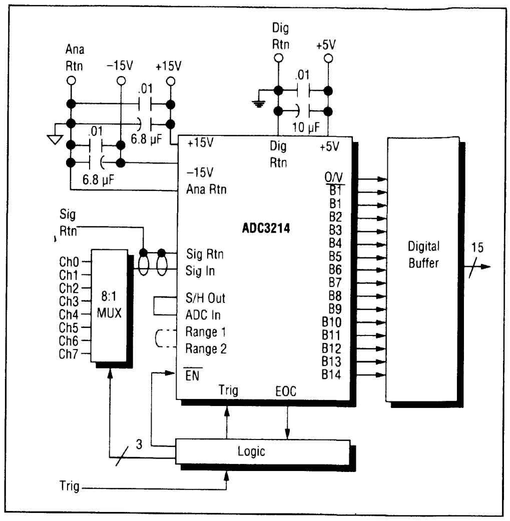


Figure 8. ADC3214-M Typical Application and Connection.

Ordering Guide

Simply Specify:

ADC3214M
14-bit Sampling A/D Converter

SP7015
DC-to-DC Converter

Analog to Digital Converters

Selection Guide

Model	Resolution	Speed	Feature	Page
ADC5041	16 to 24 Bits	1 to 100 CPS	Serial Interface	71
ADC5042	16 to 24 Bits	1 to 100 CPS	µP Interface	77
AH30217	17 Bits	300 CPS	Low Noise	85
MP2316A	16 Bits	37 CPS	FSR from ±10 mV to ±50V; Isolated with on-board DC-to-DC-Converter	91

Analog to Digital Converters

Glossary of Terms

Absolute Accuracy

A measure of the largest static difference between the actual output code and that predicted by the ideal transfer function, expressed as a percentage of full scale. In the case of a bipolar input range, e.g., −10V to +10V, the absolute accuracy is computed as a percentage of the full range, or 20V. Absolute accuracy measurements must reference a voltage standard traceable to the NIST with at least an order of magnitude lower uncertainty than the difference represented by one LSB.

A/D or ADC

An analog to digital converter is a device that accepts an analog input signal and generates the corresponding digital output code determined by its transfer function. The ideal output is accurate to ±0.5 LSB as shown by the quantizing error curve in Figure 1. A "black box" representation of an ADC is shown in Figure 2. There are a number of different ADC architectures in use. Two of the most popular are the successive approximation ADC and the integrating ADC. Speed is an inherent advantage of the successive approximation ADC. In other respects, including cost and reliability, the integrating ADC is generally superior.

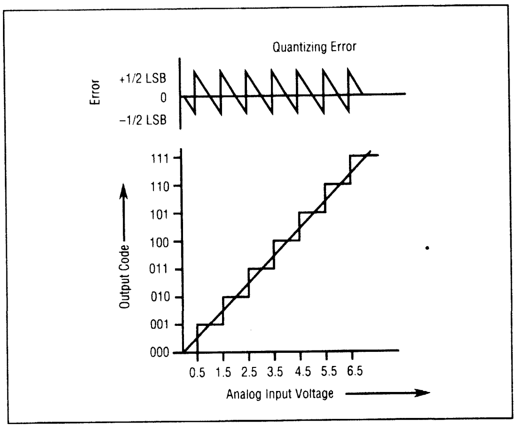


Figure 1. Theoretical Transfer Function of an ADC (first three LSBs only).

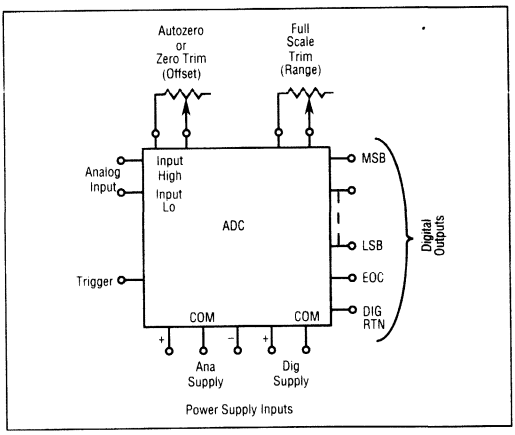
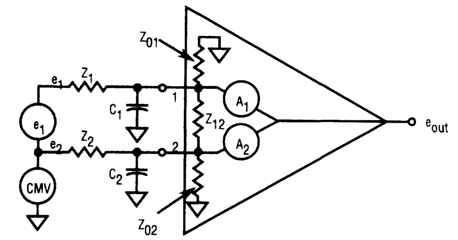


Figure 2. "Black Box" Representation of an ADC.

CMRR

The Common-Mode Rejection Ratio is a measure of the ability of an ADC with a balanced differential input to attenuate signals common to both the INPUT HI and the INPUT LO lines. See Figure 3 for configuration and formulae used to calculate CMRR.



A_1 and A_2 are the gain magnitudes between the output and inputs 1 and 2.

Z_{01} and Z_{02} are "common-mode" input impedances at terminals 1 and 2.

Z_{12} is "differential" input impedance between terminals 1 and 2.

Z_1 and Z_2 are source impedances.

C_1 and C_2 are capacitances from the inputs to ground, including input capacitance of the device itself.

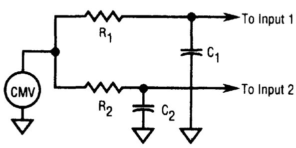
e_s = differential input signal = $(e_1 - e_2)$

CMV = common mode voltage = $e_1 - e_s$

For the device alone:

$$\text{CMRR} = 20 \log_{10} \left| \frac{1}{A_1 - A_2} \right|$$

To calculate effective external CMRR:



External Circuit Simplified

where $\frac{1}{\omega C_1} >> R_1$ and $\frac{1}{\omega C_2} >> R_2$

and $R_1 - R_2 = \Delta R$ and $C_1 - C_2 = \Delta C$

$$\text{then CMRR} \cong 20 \log_{10} \left| \frac{1}{\omega(R_1C_1 - R_2C_2)} \right|$$

$$\text{or CMRR} \cong 20 \log_{10} \left| \frac{1}{\omega(R_1\Delta_C + C_1\Delta_R)} \right|$$

Figure 3. Common-Mode Rejection Configurations and Basic Formulae.

Conversion Time

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant.

Differential Non-Linearity

A parameter that measures the difference between the theoretically uniform voltage bandwidth corresponding to a given code and the worst case actual voltage bandwidth for a given code. It is expressed either as a percentage of the ideal voltage bandwidth or as a fraction of an LSB. Figure 4 demonstrates differential nonlinearity.

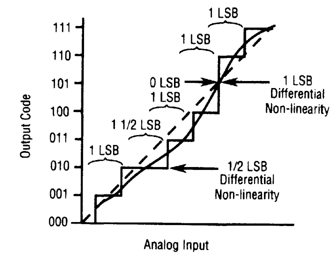


Figure 4. Differential Non-Linearity.

Gain

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

Integral Non-Linearity

A measure of the maximum deviation of the output digital codes from the best-fit straight line through the transfer function, expressed as a percentage of the full scale range. A least squares algorithm is used to determine best fit.

Integrating ADC

The integrating ADC uses a converter architecture with inherent advantages over successive-approximation ,including: lower cost for a given resolution, accuracy, linearity and stability; inherent monotonicity; high NMRR; true averaging of the signal during conversion; and the ability to autozero before every conversion cycle. The only real disadvantage is speed.

As Figure 5 shows, the conversion is accomplished in two integration phases. Because of this, it is often called a "dual slope" integrating converter. Operation is as follows:

1. In the first phase of the conversion a clock pulse generator is started and the unknown analog input signal, E_{in} charges the integrator for a fixed time interval, N_S. At the end of the time interval the charge on the integrator is proportional to E_{in}.

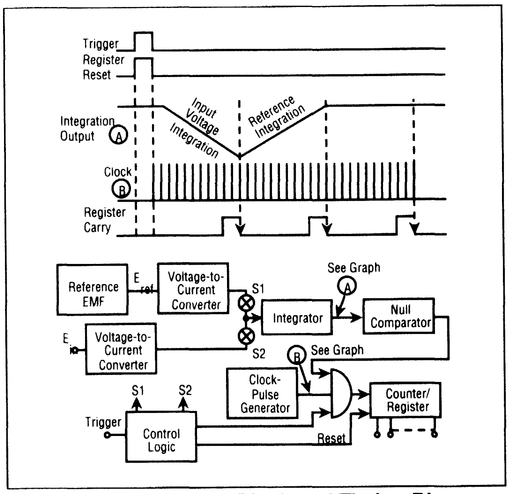


Figure 5. Fundamental Block and Timing Diagrams of Dual-Slope Integrating A/D Converter.

2. In the second phase the clock is reset and an internal standard reference voltage of opposite polarity, E_{ref}, is substituted for the input signal. This discharges the integrator, at a known rate, to zero. The time it takes to discharge the integrator, N_R, is proportional to the input signal: $N_R = E_{in}/E_{ref}) \times N_S$.

Since E_{ref} and N_S are fixed by the design, N_R will be linearly proportional to E_{in} and easily can be scaled to read directly.

As long as the components of the integrator and the clock-counter have good short-term stability, changes in their values do not decrease accuracy because both charging and discharging are affected to the same degree.

Integrating converters have a zero offset error which can be corrected by an autozeroing function. This is done by shorting the input electronically between conversions and storing the resultant integrator output on a capacitor. This stored voltage is fed back during conversion. A dual-slope integrating converter with autozeroing is called a "three-phase" or "three-step" converter: 1) autozero; 2) ramp up; 3) ramp down.

Subranging ADC

This uses an architecture that achieves high speed throughput approaching that of a flash converter with high (14- to 18-bit) resolution.

Figure 6 shows a very high speed, 16-bit resolution subranging converter. It uses a very fast, ultra-stable, 10-bit flash ADC; the first 9 MSBs of an ultra-linear, high speed 16-bit linear DAC; and switch-control logic.

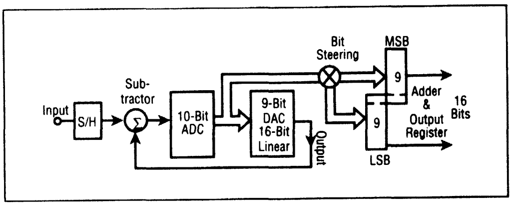


Figure 6. Subranging A/D Converter Architecture.

Monotonicity

Monotonicity is a characteristic that describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 7 demonstrates non-monotonic behavior.

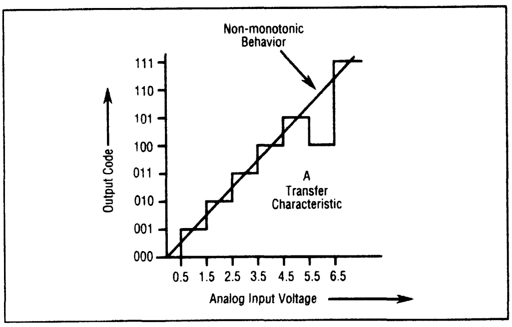


Figure 7. Non-Monotonic Behavior.

NMRR

NMRR is the abbreviation for normal mode rejection ratio. NMRR is a measure of the ability of a converter to attenuate unwanted signals, particularly noise at line frequency and its harmonics. As it pertains to an ADC it is the ratio of the transfer function of the signal component of interest to the transfer function of unwanted signal components (noise, line frequency pickup, etc.) as a function of frequency. It is expressed in decibels as follows:

$$NMRR = 20 \log_{10} (K(f_0)/K(f))$$

where $K(f_0)$ is the transfer function e_{out}/e_{in} at the frequency of the signal component of interest; f_0 is usually either 0 (DC) or a frequency consistent with the highest rate of change of the sampled input signal; and K(f) is the transfer function for the frequency at which NMRR is calculated — typically an integral multiple of the line frequency. Figure 8 shows NMRR as a function of frequency for a typical A/D converter.

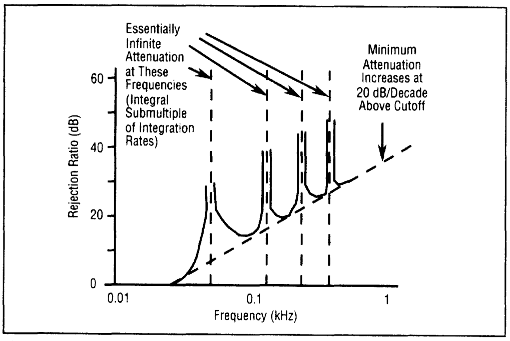


Figure 8. NMRR vs. Frequency of a Typical Integrating ADC.

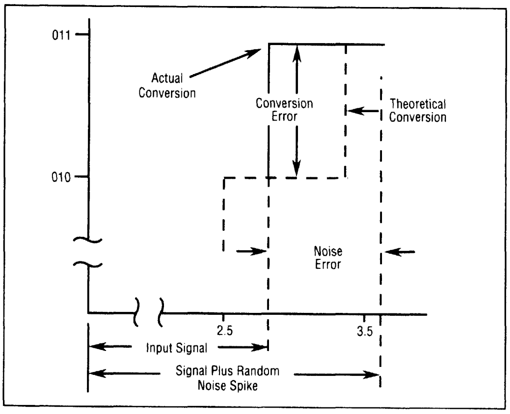


Figure 9. Effect of Noise on Conversion Accuracy.

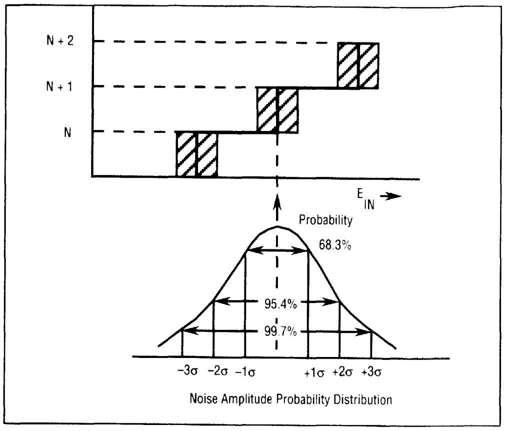


Figure 10. How Noise Affects Output-Code Transitions.

Percent of Time RMS Noise Level is Exceeded in Either Direction	Percent of Time RMS Noise Level is Exceeded in One Direction	Peak-to-Peak Noise Level
31.8%	15.9%	±1σ (2 x RMS)
20%	10%	±1.64σ (3.3 x RMS)
4.6%	2.3%	±2σ (4 x RMS)
0.3%	0.15%	±3σ (6 x RMS)
0.02%	0.01%	±3.89σ (7.8 x RMS)

Figure 11. Probability Table for Figure 10.

Noise Errors

These are errors in the output code caused by the presence of signals other than the one the ADC is trying to measure (see Figure 9). There are four main types of noise: 1) power line frequency (common mode); 2) electrical interference on the input lines (normal mode); 3) noise generated by the signal conditioning circuitry; and 4) noise generated by the ADC during the conversion process. Common mode noise can be filtered out by the integrator or by signal conditioners in the front end. Normal mode noise can usually be reduced by low pass filtering. Internally generated noise is inherent to the converter and tens to be random in nature.

The characteristics of random noise can be described by statistical measures using the Gaussian distribution function and the dispersion value (sigma). See Figure 10. Noise generated by the ADC is specified over ±3σ in μV RMS. This number can be used to calculate the percentage of time during which the noise level will exceed the 1-bit threshold and cause an incorrect output code. The table in Figure 11 shows that if the 1-bit threshold is greater than the ±3σ noise level (p-p threshold = 6 x RMS noise level), a 1-bit or greater code error of either polarity will occur less than 0.3% of the time; a unipolar error will occur less than 0.15% of the time.

Nominal Digital Levels

Digital output signal level convention. This is typically binary or tristate, standard TTL, ECL, etc., or two specific voltage ranges.

Output Code

The output of an ADC may be one of a number of binary codes. The various codes include: unipolar binary, offset binary, one's complement and two's complement. Examples of these codes are shown in Figure 12, for a 12-bit device.

Unipolar Binary:				
For a device with a nominal FSR of 0 to 10V,				
V_{max}	=	111 111 111 111	=	+9.9976V,
V_{min}	=	000 000 000 000	=	0.0000V.
Offset Binary:				
For a device with a nominal FSR of −10V to +10V,				
$V_{max\ pos.}$	=	111 111 111 111	=	+9.9951V,
$V_{midrange}$	=	100 000 000 000	=	0.0000V,
$V_{max\ neg.}$	=	000 000 000 000	=	−10.0000V.
One's Complement:				
For a device with a nominal FSR of −10V to +10V,				
$V_{max\ pos.}$	=	111 111 111 111	=	+9.9951V,
$V_{midrange}$	=	{100 000 000 000 / 011 111 111 111}	=	0.0000V,
$V_{max\ neg.}$	=	000 000 000 000	=	-9.9951V.
Two's Complement:				
For a device with a nominal FSR of −10V to +10V,				
$V_{max\ pos.}$	=	011 111 111 111	=	+9.9951V,
$V_{midrange}$	=	000 000 000 000	=	0.0000V,
$V_{max\ neg.}$	=	100 000 000 000	=	−10.0000V.

Figure 12. Most Common Binary Codes.

Parallel Threshold (Flash) ADC

The flash converter uses an architecture that achieves very fast conversions. The input signal is simultaneously applied to a large number of comparators each of which represents a successively higher LSB step. The output of the comparators is decoded to a binary value representing the highest step level attained. A block diagram of a 4-bit flash converter is shown in Figure 13.

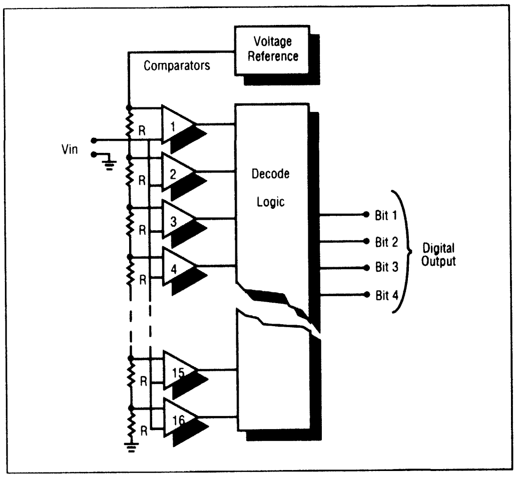


Figure 13. "Flash" A/D.

Because the number of components rises exponentially as the number of bits of resolution increases, the practical implementation of this architecture is limited to 8 bits. Resolution can be significantly increased, without an exponential increase in the circuitry, by performing a sequencing operation: flash encode the signal to yield outputs for the MSBs; convert the MSBs to an analog value and subtract that from the original input; flash encode the new input through a similar circuit to yield outputs for the LSBs.

Power Supply Coefficients

Also stated as power supply rejection ratio (PSRR), these specifications indicate how the power supply voltage affects various parameters of the ADC, e.g., ±0.001% per 1% change in power supply voltage.

Quantizing Error

The conversion error equal to the smallest quantization level of the converter, ±0.5 LSB. This error is demonstrated in Figure 1.

Relative Accuracy

This is a measure of the largest deviation of the converter's actual transfer function from the best straight line approximation of the actual transfer function, expressed as a percentage of full scale range. It comprises errors due to linearity, drift and circuit component tolerances:

e.g., ±0.005% of FSR.

Resolution — Actual Vs. Available

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes. Excessive internal noise and/or component drift can exclude the possibility of obtaining some output codes, reducing the actual resolution.

Successive Approximation ADC

The successive approximation converter uses an architecture with inherently high throughput rate that converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

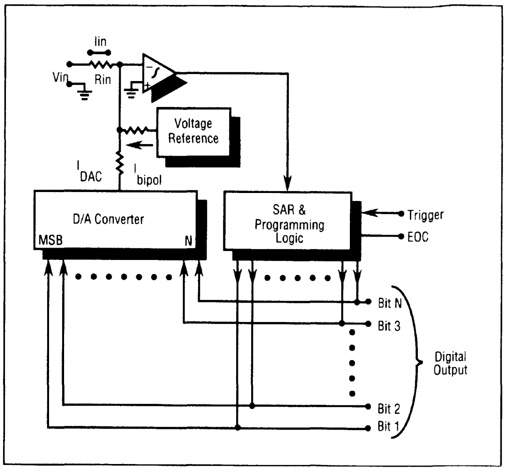


Figure 14. Block Diagram of a Successive Approximation A/D.

Temperature Coefficients

Changes in the operating temperature can affect a number of parameters, including zero offset, gain and differential linearity. The temperature coefficient, or tempco, of one of these parameters is computed as the change in that parameter over a specified temperature range divided by the number of degrees in that temperature range. This yields an average tempco over the temperature range, not the worst case. Analogic tempco specifications are conservative and generally may be considered worst case values.

Throughput

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rated performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time, and the conversion time.

Zero Offset

The input voltage required to yield an output code corresponding to zero. Provision is normally made to allow the user to adjust the zero offset.

Bitweight Conversion Table

Binary Bits	Codes	Percent Per Code	ppm Per Code	LSB Value 10V FS	Theoretical S/N Ratio in dB	Dynamic Range in dB
1	2	50.0	500000	5.0	7	6
2	4	25.0	250000	2.5	13	12
3	8	12/5	125000	1/25	19	18
4	16	6.25	62500	0.625	25	24
5	32	3.125	31250	0.3125	31	30
6	64	1.5625	15625	0.15625	37	36
7	128	0.78125	7812.5	0.078125	43	42
8	256	0.390625	3906.2	0.0309625	49	48
9	512	0.1953125	1953.1	0.0195313	55	54
10	1024	0.0976566	976.57	0.0097656	61	60
11	2048	0.0488281	488.28	0.0048828	67	66
12	4096	0.0244140	244.14	0.0024414	74	72
13	8192	0.0122070	122.07	0.0012207	80	78
14	16384	0.0061035	61.035	0.0006104	86	84
15	32768	0.0030517	30.517	0.0003052	92	90
16	65536	0.0015258	15.258	0.0001526	98	96
17	131072	0.0007629	7.629	0.0000763	104	102
18	262144	0.0003814	3.814	0.0000381	110	108
19	524288	0.0001907	1.907	0.0000191	116	114
20	1048576	0.0000953	0.953	0.0000095	122	120
21	2097152	0.0000476	0.476	0.0000048	128	126
22	4194304	0.0000238	0.238	0.0000024	134	132
23	8388608	0.0000119	0.119	0.0000012	140	138
24	16777216	0.0000059	0.059	0.0000006	146	144

ADC5041

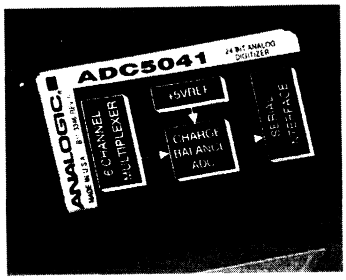
Serial-Interfaced, 24-Bit, 6-Channel, A/D Digitizer

For Use in Applications Requiring Very Wide Dynamic Range

Introduction

The ADC5041 is a low-cost 6-channel digitizer with programmable resolution from 16 to 24 bits. It is designed for use in applications requiring very wide dynamic range, such as multipoint process control, temperature recorders, strain gauge measurement, load cell digitizers, and chromatography. Unlike traditional dual or multislope devices, the ADC5041, coupled with a host microprocessor, provides superior flexibility and performance. With a ±5V input range and 24-bit resolution, the ADC5041 provides 144 dB of dynamic range, which eliminates the PGA requirements in most high-precision measurements applications, reduces parts count and cost, and improves overall circuit performance. The input amplifier is user configurable, allowing for additional gain if required.

The ADC5041 consists of a 6-channel multiplexer, an input amplifier, a precision +5V reference, a multislope charge-balanced integrating A/D converter, and a serial UART interface. Available in a 40-pin DIP package, the ADC5041 uses the latest surface mount technology to provide a cost-effective, high-performance part offering ±0.00075% linearity and a low 10 µV RMS input referred noise.



Features

- ❑ 16- to 24-Bit Resolution
  24 Bits @ 1 CPS
  16 Bits @ 100 CPS
- ❑ 6-Channel Multiplexer
- ❑ User-Configurable Input Amplifier
- ❑ Low Cost
- ❑ Serial UART Interface
- ❑ 40-Pin DIP Package
- ❑ Charge Balance Architecture
- ❑ On-Board Reference

Applications

- ❑ Chemical Process Control
- ❑ Chromatography
- ❑ Data Loggers
- ❑ Load Cell Digitizers
- ❑ RTD Measurement
- ❑ Strain Gauge
- ❑ Surface Profile Indicators
- ❑ Thermocouple Measurements

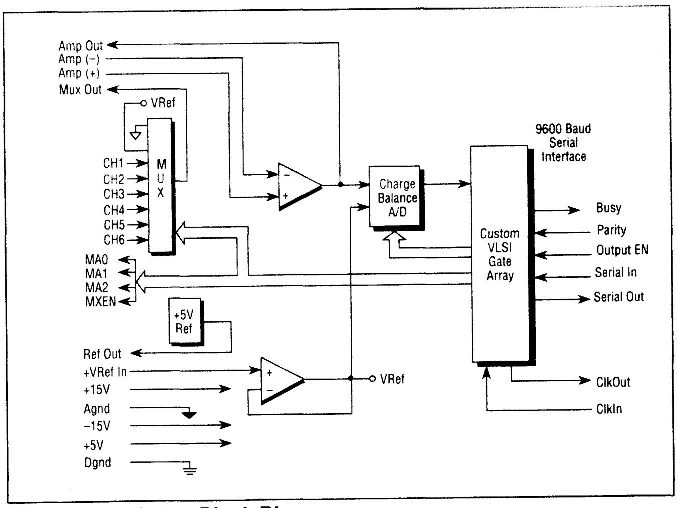


Figure 1. ADC5041 Block Diagram.

ADC5041

Specifications[1]

ABSOLUTE MAXIMUM RATINGS

Analog Input
±Vref ±0.3 volts

Digital Input
+Vd +0.2 volts

Reference Input
0V to +5.3V

ANALOG INPUTS

Analog Input Range
–5 volts to +5 volts

Input Amplifier Impedance
100 MΩ/10 pF

Input Amplifier Bias Current
50 pA

Input Amplifier Configuration
User Configurable

Input Amplifier Maximum Output Loading
10 kΩ Min.

Channels
6

DIGITAL INPUTS

Logic Level
LSTTL/CMOS Compatible

Logic "0"
0.8 volts Max.

Logic "1"
2.0 volts Min.

Clock Input Frequency
3.072 MHz 60/40 Duty Cycle Typ.

Minimum Reset Pulse Width
50 ns Min. Negative-Going Pulse

Loading CMOS Input Loading
10 pF Typ.

DIGITAL OUTPUTS

Compatibility
LSTTL

Logic "0"
0.4 volts Max. @ 4 mA

Logic "1"
3.7 volts Min. @ 4 mA

Output Loading
4 mA Max.

Digitized Data Output
Unipolar Magnitude Format

Busy
Active High Indicates Conversion in Progress

INTERNAL REFERENCE

Reference Output Voltage
+5 volts ±5 mV

Output Current [2]
2 mA

Temperature Stability
±15 ppm/°C

Reference Input Impedance
100 MΩ/10 pF

TRANSFER CHARACTERISTICS

Relative Accuracy
±0.00075% FSR Max.

Noise [3]
10 μV RMS

Normal Mode Rejection [4]
80 dB Min.

Conversion Rate
See Table 2

STABILITY

Uncalibrated Zero Drift
±20 ppm/°C Max.

Uncalibrated Full Scale Drift
±10 ppm/°C Max.

Calibrated Zero Drift [5]
±0.7 ppm Max. Absolute

Calibrated Full Scale Drift [5]
±0.34 ppm Max. Absolute

Warmup Time
3 Minutes Max.

POWER REQUIREMENTS

Voltage
+VA
+11.5 volts to +15.75 volts
–VA
–11.5 volts to –15.75 volts
+VD
+4.75 volts to +5.25 volts

Current
+VA
18 mA Typ.
–VA
12 mA Typ.
+VD
4 mA Typ.

Power
500 mW Typ.

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature
0°C to 70°C

Storage Temperature
–25°C to +125°C

Relative Humidity
85% Non-condensing to +70°C

NOTES:

1. Unless otherwise noted, all specifications apply at 25°C ambient with power supplies at ±15 and +5 volts.
2. Reference load must remain stable during conversion.
3. Measured at 22-bit resolution with 60 Hz line cycle integration.
4. Line cycle must equal signal integration time (Tint), ±0.02%. Normal mode rejection occurs at conversion speeds which result in integration times that are multiples of the AC line frequency (see conversion timing chart).
5. Absolute errors assume 1/4°C/minute temperature drift, with offset and gain calibrations performed after each input signal conversion. The errors are absolute to the reference that is used for the calibration.

Specifications subject to change without notice.

ADC5041 INTERFACING

Signal Input Connections

The ADC5041, with its internal 6-channel multiplexer and uncommitted amplifier, can be configured for virtually any type of front-end processing. Figure 2 shows two possible single-ended amplifier configurations. The front-end flexibility of the ADC5041 allows for extending the channel capacity to 14 single-ended or 6 differential channels as shown in Figures 3a and 3b.

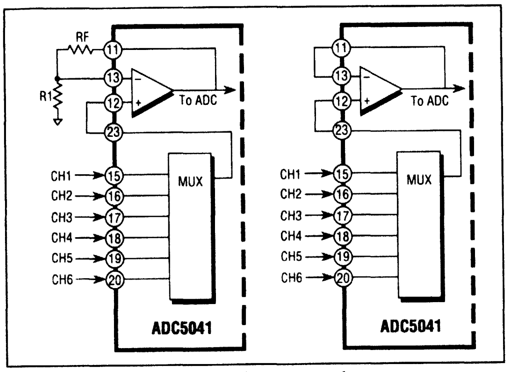


Figure 2. Single-Ended Configurations.

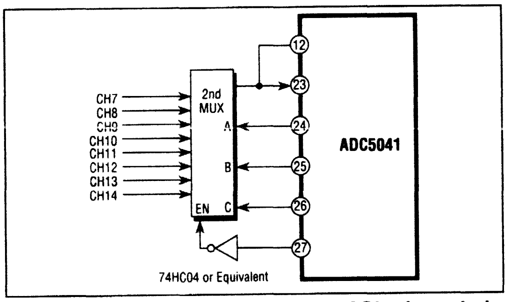


Figure 3a. Extending the Number of Single-ended Input Channels.

Multiplexer Address Outputs

The multiplexer address outputs reflect the internal multiplexer address. These outputs are useful for connecting an additional multiplexer to extend the number of channels or to provide differential operation. Figure 3 shows two possible configurations. Note that the multiplexer enable output is inverted when using a second multiplexer to add channels.

Reference Connections

The ADC5041 contains an on-board +5 volt reference. This reference is brought out on Pin 22 and can drive loads up to 2 mA (any loading on reference should be static). The reference output can be looped around to

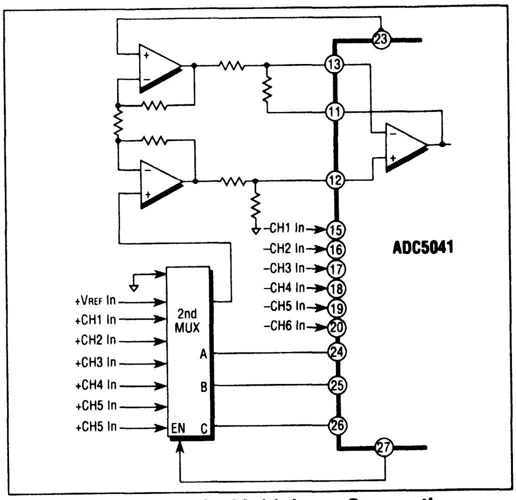


Figure 3b. Differential Multiplexer Connections.

the reference input (Pin 21) and can also be used as the host system's reference. Alternatively, the reference input can be driven from an externally supplied +5 volt reference as long as the external reference is stable and quiet (Tc <25 ppm/°C and noise <4 µV pk-pk [0.1 to 10 Hz]).

Clock Input Connections

The external 3.072 MHz clock must be supplied from a CMOS can oscillator as shown in Figure 4. The clock input is divided by two internally.

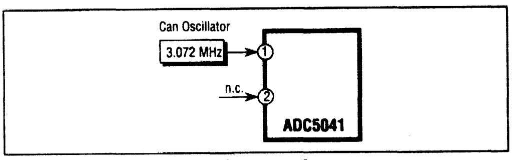


Figure 4. Clock Input Connections.

50/60 Hz Select Input

The signal integration period (Tint) as shown in Figure 9 can be based on a 20 ms (50 Hz) or 16.667 ms (60 Hz) line cycle for optimum rejection of AC line noise. This rejection improves as more line cycles are used for integration periods (see Figure 10). A logic low on this input will select 60 Hz integration periods.

Reset Input

The reset input when taken to a logic "zero" resets all internal logic and sets the busy output to a logic high. When taken back to a logic "one", an internal counter

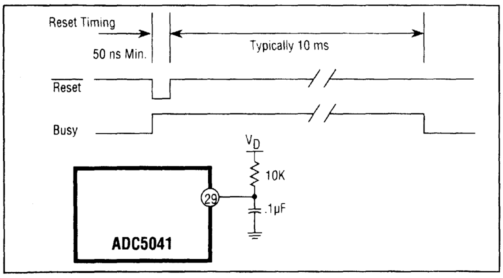


Figure 5. Reset Timing and Connections.

counts 16384 internal clock cycles, providing a 10 ms stabilization time for the analog circuitry to settle. The reset input has a Schmitt trigger buffer allowing for the use of a simple RC combination to provide for a power-up reset. Figure 5 shows a typical reset connection and timing.

Serial UART Interfacing with the ADC5041

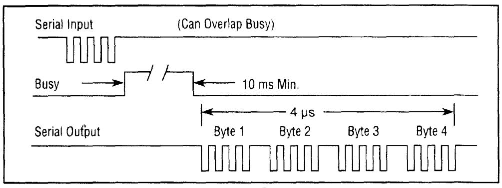


Figure 6. Serial Input and Output Timing.

The ADC5041 contains a command register and four output data registers. All data in and out of the ADC5041 registers are transferred using the 9600 baud serial input and output pins. The registers and their bit definitions are shown in Figures 7 and 8.

Conversions and input multiplexer channels are selected when the command register is updated following a valid serial transmission (invalid transmission occurs when the incoming parity does not agree with the selection via Pin 6 or if a framing error occurs). Following the reception of a serial byte, the appropriate channel is selected and, if bit 7 = 1, a digitization is started.

Digitized data residing in the four data registers is sent out as a four-byte frame immediately following a digitization. Figure 6 shows this timing. Figure 7 shows the command register definition for multiplexer channels and resolution (integration times).

ADC5041 Operating Overview

The ADC5041 is a variable resolution digitizer with an on-board multiplexer and reference. When used in conjunction with a host microprocessor, the ADC5041 provides a low-cost, accurate way to convert low level signals to a digital format.

The ADC5041 achieves its superior performance by use of a very linear multislope charge balance integrator and a custom VLSI IC. The digitization process starts with a serial in command (see Figure 9). Following a 10 µs delay to allow for multiplexer settling time, the input signal is integrated for time Tint. During this time, packets of energy are periodically removed. This architecture keeps the integrator output "ratcheting" around on a constant voltage helping to optimize this circuit for linearity, low noise, and speed. After this time, the input signal is disconnected and a reference integration follows for approximately 5 ms. During both

Mode	D7	D6	D5	D4	D3	D2	D1	D0
16-Bit	1*	X	X	X	X	0	0	0
18-Bit	1*	X	X	X	X	0	1	0
20-Bit	1*	X	X	X	X	0	1	1
22-Bit	1*	X	X	X	X	1	0	0
24-Bit	1*	X	X	X	X	1	1	1

Figure 7a. Resolution Table.

*NOTE: D7 is the conversion enable bit. To select channels without a conversion set D7 = 0.

CH #	D7	D6	D5	D4	D3	D2	D1	D0
Gnd	1*	0	0	0	0	X	X	X
VRef	1*	0	0	0	1	X	X	X
CH 1	1*	0	0	1	0	X	X	X
CH 2	1*	0	0	1	1	X	X	X
CH 3	1*	0	1	0	0	X	X	X
CH 4	1*	0	1	0	1	X	X	X
CH 5	1*	0	1	1	0	X	X	X
CH 6	1*	0	1	1	1	X	X	X
No CH	1*	1	X	X	X	X	X	X

Figure 7b. Channel Selection Table.

Data Register 1 (A0 = 0, A1 = 0)

D7	D6	D5	D4	D3	D2	D1	D0
Valid R x Data 0 = Error	MUX EN 1 = Disable 0 = Enable	MA2	MA1	MA0	Parity Error 1 = Error	Data Bit 25 (MSB)	Data Bit 24

Data Register 2 (A0 = 1, A1 = 0)

D7	D6	D5	D4	D3	D2	D1	D0
Data Bit 23	Data Bit 22	Data Bit 21	Data Bit 20	Data Bit 19	Data Bit 18	Data Bit 17	Data Bit 16

Data Register 3 (A0 = 0, A1 = 1)

D7	D6	D5	D4	D3	D2	D1	D0
Data Bit 15	Data Bit 14	Data Bit 13	Data Bit 12	Data Bit 11	Data Bit 10	Data Bit 9	Data Bit 8

Data Register 4 (A0 = 1, A1 = 1)

D7	D6	D5	D4	D3	D2	D1	D0
Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)

Figure 8. Output Data Byte Registers.

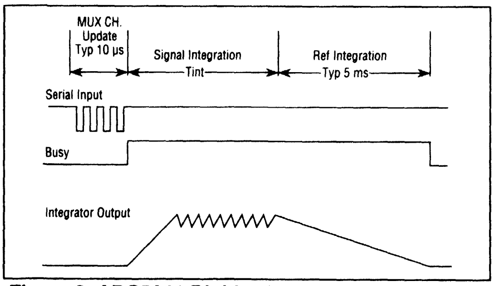


Figure 9. ADC5041 Digitization Timing.

integration cycles, a 26-bit counter keeps track of the accumulated charge due to the input signal. At the end of the reference integration, the counter's output is available via the microprocessor interface. Digitization times along with their associated Tints are shown in Figure 10.

Resolution	Tint (Line Cycles) n	CPS (50/60 Hz)
16 Bits	1/4	100/100
18 Bits	1	40/46
20 Bits	4	12/13
22 Bits	16	3/3.6
24 Bits	64	1.2/.93

Note: Line cycle at 60 Hz = 16.667 ms; 50 Hz = 20 ms

Figure 10. Digitization Times Versus Resolution.

ADC5041 Output Data Format

The output data registers are updated with the contents of a 26-bit counter which keeps track of the input signal charge accumulated during the digitization process. This data will contain a span and offset error, which is easily removed by the host microprocessor.

The span is defined as the difference between the counts due to a minus full scale input (–5V) and the counts due to a plus full scale input (+5V). Note that for the ADC5041, a –5V input produces the most counts and a +5V signal produces the least counts. The ideal span is normally 2n, where n = the resolution selected; however, the actual span in the ADC5041 will be greater than the ideal span. This span error actually results in a slight increase in resolution and need only be calibrated out. It has no other effect on the resulting data.

The offset error is due to an offset voltage added to the input signal during signal integration. This offset has the effect of producing a larger number of counts for a given input than would normally be expected (this is why a 26-bit counter is necessary even though the maximum resolution is 24 bits). Since it is a true offset, these additional counts are constant for any given input signal and thus contribute no gain error. They are simply subtracted from the final result with the host microprocessor.

Calibration of ADC5041 Output Data

Calibration of the output data to eliminate the above-mentioned offset and span errors is very simple. The offset counts are quantified by digitizing a 0 volt input. This can be either the ADC5041's Offset Channel or any other multiplexer channel connected to signal ground. The span error is measured by digitizing a known voltage near either plus or minus full scale. This can be either the ADC5041's Reference Channel or a stable input on any other multiplexer channel. Using a calibration algorithm in the host microprocessor, such as the one shown in Figure 11, the resulting output data is converted to volts and its absolute accuracy follows the reference used.

There are variations that can be useful. Two references can be used for the span reading, one at –FS and one at +FS (where Vref = (+FS) - (–FS). This has the advantage of correcting over the full dynamic range, but requires two multiplexer channels devoted to a reference.

Since the span and offset errors of the ADC5041 are time- and temperature-sensitive, calibration should be done on a periodic basis.

The frequency of calibration is application specific and should be based on the stability of the operating environment and resolution selected. However, it should always be done at power-up and until the ambient operating conditions have stabilized.

The calibration should be done periodically to remove errors associated with a change in the ambient temperature or time. The optimum frequency is determined by system characteristics and operating environment.

A 1°C change in temperature represents a worst-case 30 ppm (combined offset and gain TC) change or 2 LSBs at 16 bits.

To maintain an absolute accuracy TC of ±1 LSB, calibration is required for every 0.5°C change in temperature.

$$\text{ppm/LSB @ 16 bits} = \frac{1 \times 10^6}{2^n} = 15.3 \text{ ppm}$$

ADC5041 Pin Assignment

PIN #	FUNCTION	DESCRIPTION
1	X1/CLKIN	3.072 MHz Clock/Crystal Input
2	X2/CLKOUT	3.072 MHz Crystal Input
3	OENI	Active Low Input Used to enable Tri-State Serial Output
4	SOUT	9600 Baud Serial Output
5	SIN	9600 Baud Serial Input
6	PARI	Active High Input Selects Even Parity Logic Low Input Selects No Parity
7	N.C.	
8	+VA	+11.5 to 15.75 volt Input
9	–VA	–11.5 to –15.75 volt Input
10	AGND	Analog Ground
11	AMP OUT	Output of Internal Amplifier
12	AMP+	Non-inverting Input of Internal Amplifier
13	AMP–	Inverting Input of Input Amplifier
14	SIG GND	Signal Ground
15	CH1	Multiplexer Input Channel 1
16	CH2	Multiplexer Input Channel 2
17	CH3	Multiplexer Input Channel 3
18	CH4	Multiplexer Input Channel 4
19	CH5	Multiplexer Input Channel 5
20	CH6	Multiplexer Input Channel 6
21	REF IN	5 volt Reference Out
22	REF OUT	Internal 5 volt Reference Out
23	MUX OUT	Internal Multiplexer Output
24	MA0	Active High Internal Multiplexer Address Output
25	MA1	Active High Internal Multiplexer Address Output
26	MA2	Active High Internal Multiplexer Address Output
27	MXEN	Active High Internal Multiplexer Enable Output
28	BUSY	Active High Output Indicates Digitization Active
29	RESET	Active Low Input Resets All Logic
30	50/60 SELECT	Active Low Selects 60 Hz Integration Line Cycles
31	DGND	Digital Ground
32	$+V_D$	+5 volts
33	N.C.	
34	N.C.	
35	N.C.	
36	N.C.	
37	N.C.	
38	N.C.	
39	N.C.	
40	N.C.	

$$\text{VOUT (volts)} = (\text{VIN COUNTS-OFFSET COUNTS}) * \frac{\text{VREF (volts)}}{(\text{REF COUNTS-OFFSET COUNTS})}$$

Figure 11. Calibration Formula.

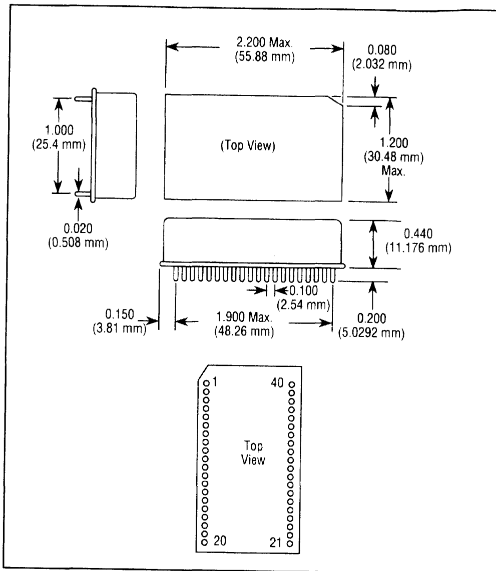


Figure 12. Outline Dimensions.

Ordering Guide

Specify: **ADC5041 – Full UART Interfacing**
ADC5042 – µP Interfacing

ADC5042

μP Compatible, 24-Bit, 6-Channel, A/D Digitizer

For Use in Applications Requiring Very Wide Dynamic Range

Introduction

The ADC5042 is a low-cost 6-channel digitizer with programmable resolutions from 16 to 24 bits. It is designed for use in applications requiring very wide dynamic range, such as multipoint process control, temperature recorders, strain gauge measurement, load cell digitizers, and chromatography. Unlike traditional dual or multislope devices, the ADC5042, coupled with a host microprocessor, provides superior flexibility and performance. With a ±5V input range and 24-bit resolution, the ADC5042 provides 144 dB of dynamic range, which eliminates the PGA requirements in most high-precision measurement applications, reduces parts count and cost, and improves overall circuit performance. The input amplifier is user configurable, allowing for additional gain if required.

The ADC5042 consists of a 6-channel multiplexer, input amplifier, a precision +5V reference, a multislope charge balanced integrating A/D converter, and all the required interface logic for coupling to a host microprocessor. Available in a 40-pin DIP package, the ADC5042 uses the latest surface mount technology to provide a cost-effective, high-performance part offering ±0.00075% linearity and a low 10 μV RMS input referred noise.

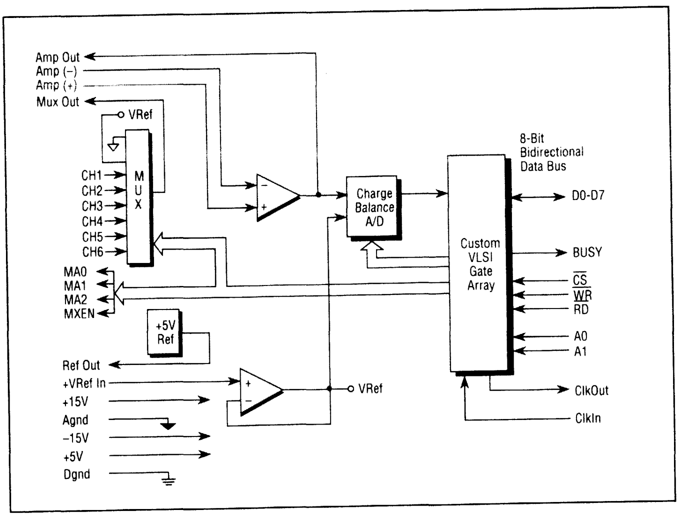


Figure 1. ADC5042 Block Diagram

Features

- ❑ 16- to 24-Bit Resolution
  24 Bits @ 1 CPS
  16 Bits @ 100 CPS
- ❑ 6-Channel Multiplexer
- ❑ On-Board Reference
- ❑ User-Configurable Input Amplifier
- ❑ Low Cost
- ❑ Full μP Interface
- ❑ 40-pin DIP Package
- ❑ Charge Balance Architecture

Applications

- ❑ Chemical Process Control
- ❑ Chromatography
- ❑ Data Loggers
- ❑ Load Cell Digitizers
- ❑ RTD Measurement
- ❑ Strain Gage
- ❑ Surface Profile Indicators
- ❑ Thermocouple Measurements

ANALOGIC®
The World Resource for Precision Signal Technology

ADC5042

Specifications[1]

ABSOLUTE MAXIMUM RATINGS

Analog Input
±Vref ±0.3 volts

Digital Input
+Vd +0.2 volts

Reference Input
0V to +5.3 V

ANALOG INPUTS

Analog Input Range
-5 volts to +5 volts

Input Amplifier Impedance
100 MΩ/10 pF

Input Amplifier Bias Current
50 pA

Input Amplifier Configuration
User-Configurable

Input Amplifier Maximum Output Loading
10 kΩ Min.

Channels
6

DIGITAL INPUTS

Logic Level
LSTTL/CMOS Compatible

Logic "0"
0.8 volts Max.

Logic "1"
2.0 volts Min.

Clock Input Frequency
3.072 MHz 60/40 Duty Cycle Typ.

Minimum Reset Pulse Width
50 ns Min. Negative Going Pulse

Loading CMOS Input Loading
10 pF Typ.

DIGITAL OUTPUTS

Compatibility
LSTTL

Logic "0"
0.4 volts Max. @ 4 mA

Logic "1"
3.7 volts Min. @ 4 mA

Output Loading
4 mA Max.

Digitized Data Output
Unipolar Magnitude Format

Busy
Active High Indicates Conversion in Progress

INTERNAL REFERENCE

Reference Output Voltage
+5 volts ±5 mV

Output Current[2]
2 mA

Temperature Stability
±15 ppm/°C

Reference Input Impedance
100 MΩ//10 pF

TRANSFER CHARACTERISTICS

Relative Accuracy
±0.00075% FSR Max.

Noise
10 μV RMS[3]

Normal Mode Rejection[4]
80 dB Min.

Conversion Rate
See Table 2

STABILITY

Uncalibrated Zero Drift
±20 ppm/°C Max.

Uncalibrated Full Scale Drift
±10 ppm/°C Max.

Calibrated Zero Drift[5]
±0.7 ppm Max. Absolute

Calibrated Full Scale Drift[5]
±0.34 ppm Max. Absolute

Warmup Time
3 Minutes Max.

POWER REQUIREMENTS

Voltage

+VA
+11.5 volts to +15.75 volts

–VA
-11.5 volts to -15.75 volts

+VD
+4.75 volts to +5.25 volts

Current

+VA
18 mA Typ.

–VA
12 mA Typ.

+VD
4 mA Typ.

Power
500 mW Typ.

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature
0°C to 70°C

Storage Temperature
-25°C to +125°C

Relative Humidity
85% Non-Condensing to +70°C

Specifications subject to change without notice.

NOTES:

1. Unless otherwise noted, all specifications apply at 25°C ambient with power supplies at ±15 and +5 volts.
2. Reference load must remain stable during conversion.
3. Measured at 22-bit resolution with 60 Hz line cycle integration.
4. Line cycle must equal signal integration time (Tint), ± 0.02%. Normal mode rejection occurs at conversion speeds which result in integration times that are multiples of the AC line frequency (see conversion timing chart).
5. Absolute errors assume 1/4°C/minute temperature drift, with offset and gain calibrations performed after each input signal conversion. The errors are absolute to the reference that is used for the calibration.

ADC5042 INTERFACING

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The ADC5042, with its internal 6-channel multiplexer and uncommitted amplifier, can be configured for virtually any type of front end processing. Figure 2 shows two possible single-ended amplifier configurations. The front end flexibility of the ADC5042 allows for extending the channel capacity to 14 single-ended or 6 differential channels as shown in Figures 3a and 3b.

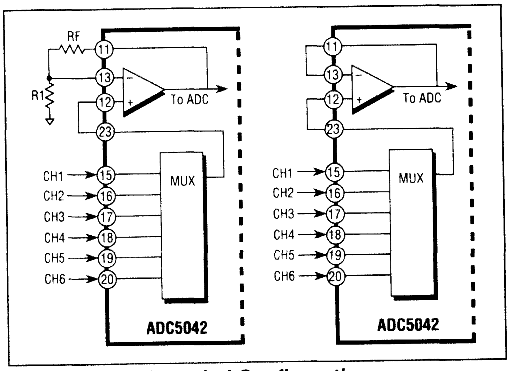

Figure 2. Single-ended Configurations.

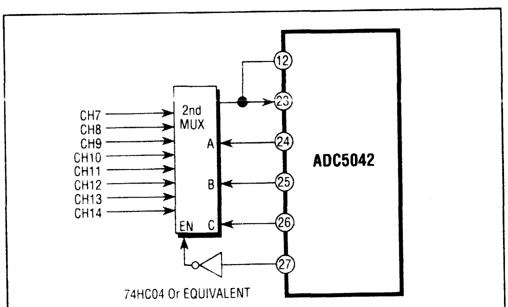

Figure 3a. Extending the Number of Single-ended Input Channels.

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Reference Connections

The ADC5042 contains an on-board +5 volt reference. This reference is brought out on Pin 22 and can drive

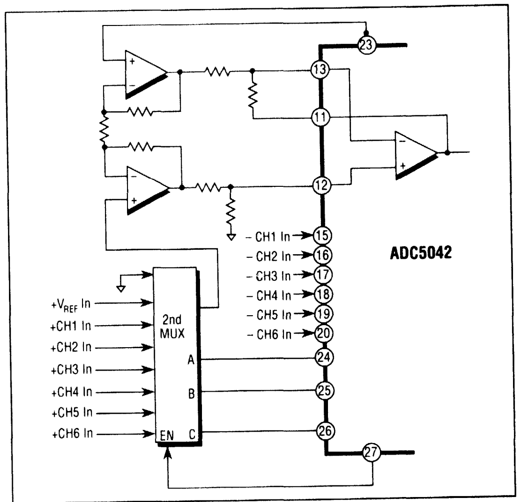


Figure 3b. Differential Multiplexer Connections.

loads up to 2 mA (any loading on reference should be static). The reference output can be looped around to the reference input (Pin 21) and can also be used as the host system's reference. Alternatively, the reference input can be driven from an externally supplied +5 volt reference as long as the external reference is stable and quiet (Tc <25 ppm/°C and noise <4 μV pk-pk [0.1 to 10 Hz]).

Clock Input Connections

The external 3.072 MHz clock must be supplied from a CMOS can oscillator as shown in Figure 4. The clock input is divided by two internally. When a can oscillator is used, it must drive the clock input with CMOS levels.

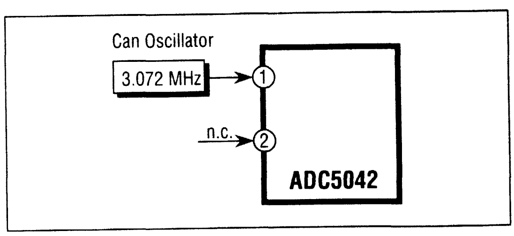


Figure 4. Clock Input Connections

50/60 Hz Select Input

The signal integration period (Tint) as shown in Figure 9 can be based on a 20 ms (50 Hz) or 16.667 ms (60 Hz) line cycle for optimum rejection of AC line noise. This rejection improves as more line cycles are used

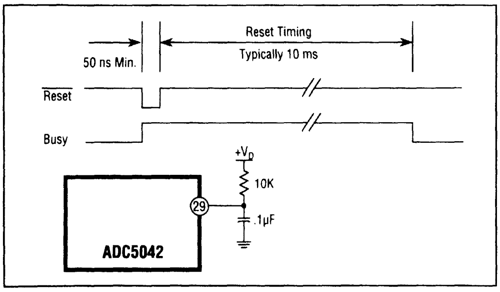


Figure 5. Reset Timing and Connections.

for integration periods (see Table 2). A logic low on this input will select 60 Hz integration periods.

Reset Input

The reset input when taken to a logic "zero" resets all internal logic and sets the busy output to a logic high. When taken back to a logic "one", an internal counter counts 16384 internal clock cycles, providing a 10 ms stabilization time for the analog circuitry to settle. The reset input has a Schmitt trigger buffer allowing for the use of a simple RC combination to provide for a power-up reset. Figure 5 shows a typical reset connection and timing.

Interfacing with the ADC5042

The ADC5042 parallel interface consists of five control lines and an 8-bit data bus. There is one command register and four data registers. Figure 7 shows the relationship between the control lines and the five internal registers.

The command register is used to select the resolution, channel number, and to enable a digitization.

The result of the digitization, which is held in an internal 26-bit counter, is available via the four data registers. Data Register 1 also contains the current multiplexer address and the status of the busy pin.

READ CYCLE TIMING REQUIREMENTS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
Trdpw	$\overline{\text{RD}}$ Pulse Width	100			ns
Tcsrd	Chip Select to $\overline{\text{RD}}$ Low	0			ns
Tcsh	Chip Select Hold Time	0			ns
Tas	Address Set Up Time	1			ns
Tah	Address Hold Time	0			ns
Tdv	Data Valid Time			70	ns
Tdh	Data Hold Time			50	ns

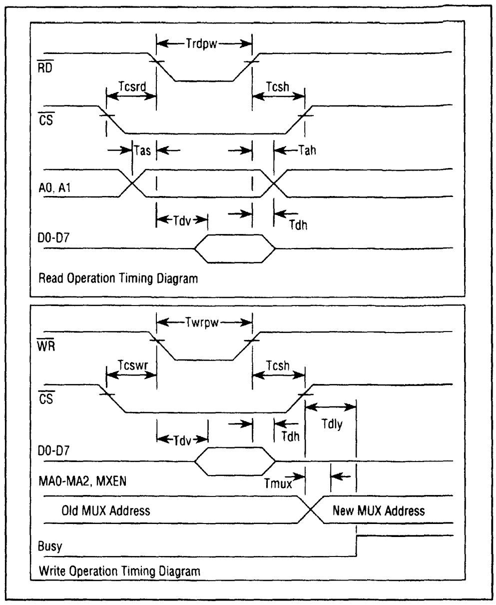


Figure 6. Read and Write Timing.

WRITE CYCLE TIMING REQUIREMENTS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
Twrpw	$\overline{\text{WR}}$ Pulse Width	100			ns
Tcswr	Chip Select to $\overline{\text{WR}}$ Low	0			ns
Tcsh	Chip Select Hold Time	0			ns
Tdly	Delay To Conversion Start		11		us
Tmux	Mux Delay Time			40	ns
Tdv	Data Valid Time			70	ns
Tdh	Data Hold Time			50	ns

Register	$\overline{\text{CS}}$	$\overline{\text{WR}}$	$\overline{\text{RD}}$	A0	A1
Command Register	0	0 to 1	1	X	X
Data Register 1 (Status) Register	0	1	0	0	0
Data Register 2	0	1	0	1	0
Data Register 3	0	1	0	0	1
Data Register 4	0	1	0	1	1

Figure 7. Register Map.

ADC5042 Command Register

The command register is written to on the positive edge of the $\overline{\text{WR}}$ input with $\overline{\text{CS}}$ at a logic low as shown in Figure 6. The format of this register is shown in Figures 8a and 8b.

Bits D0 thru D2 select one of five resolutions. Table 2 shows the relationship between signal integration time and the resolution of the digitization.

Bits D3 thru D6 select the multiplexer channel as well as its enable line. By manipulation of Bit 6, any one of eight on-board or external channels (with an externally supplied multiplexer) can be selected, previously shown in Figures 3a and 3b.

Bit 7 is the digitization enable bit. When this bit is set to a 1, a digitization will commence on the rising edge of $\overline{WR}$ (with $\overline{CS}$ held low). If this bit is logic zero, just the multiplexer address is updated when this register is written to. This is useful for changing the multiplexer and allowing for extended settling times due to high gain, external filtering, etc. In this case, rewriting the command register with D7 = 1 will then initiate a digitization.

Mode	D7	D6	D5	D4	D3	D2	D1	D0
16-Bit	1*	X	X	X	X	0	0	0
18-Bit	1*	X	X	X	X	0	1	0
20-Bit	1*	X	X	X	X	0	1	1
22-Bit	1*	X	X	X	X	1	0	0
24-Bit	1*	X	X	X	X	1	1	1

Figure 8a. Resolution table

*NOTE: D7 is the conversion enable bit. To select channels without a conversion set D7 = 0.

CH #	D7	D6	D5	D4	D3	D2	D1	D0
Gnd	1*	0	0	0	0	X	X	X
VRef	1*	0	0	0	1	X	X	X
CH 1	1*	0	0	1	0	X	X	X
CH 2	1*	0	0	1	1	X	X	X
CH 3	1*	0	1	0	0	X	X	X
CH 4	1*	0	1	0	1	X	X	X
CH 5	1*	0	1	1	0	X	X	X
CH 6	1*	0	1	1	1	X	X	X
No CH	1*	1	X	X	X	X	X	X

Figure 8b. Channel Selection table.

ADC5042 Data/Status Registers

The four data registers are selected with the A0 and A1 control inputs and are active on the data bus when the $\overline{CS}$ and $\overline{RD}$ inputs are at a logic low. Figure 8 shows the register map access, with the timing requirements shown in Figure 6.

As shown in Table 1, Data Register 1 (A1=0, A0=0) contains the status of the busy pin and the current multiplexer channel and can be read at any time during the digitization. This register also contains two of the data bits, one of which is the MSB. Data Registers 1 thru 3 contain the rest of the digitized data (for resolutions in which bits are unused, these bits are set to 0).

The data bits are updated immediately following a digitization, which can be monitored via the busy bit. The data remains buffered and valid until the next digitization overwrites the current data.

Table 1.

Data Register 1 (A0 = 0, A1 = 0)							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
A/D Status 1 = Busy 0 = Idle	MUX EN 1 = Disable 0 = Enable	MA2	MA1	MA0	Reserved	Data Bit 25 (MSB)	Data Bit 24
Data Register 2 (A0 = 1, A1 = 0)							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Data Bit 23	Data Bit 22	Data Bit 21	Data Bit 20	Data Bit 19	Data Bit 18	Data Bit 17	Data Bit 16
Data Register 3 (A0 = 0, A1 = 1)							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Data Bit 15	Data Bit 14	Data Bit 13	Data Bit 12	Data Bit 11	Data Bit 10	Data Bit 9	Data Bit 8
Data Register 4 (A0 = 1, A1 = 1)							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)

ADC5042 Operating Overview

The ADC5042 is a variable resolution digitizer with an on-board multiplexer and reference. When used in conjunction with a host microprocessor, the ADC5042 provides a low-cost, accurate way to convert low level signals to a digital format.

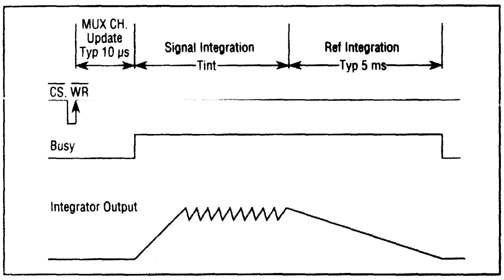


Figure 9. ADC5042 Digitization Timing.

Table 2.

Resolution	Tint (Line Cycles)^n	CPS (50/60 Hz)
16 Bits	1/4	100/100
18 Bits	1	40/46
20 Bits	4	12/13
22 Bits	16	3/3.6
24 Bits	64	1.2/.93

Note: Line cycle at 60 Hz = 16.667 ms; 50 Hz = 20 ms

The ADC5042 achieves its superior performance by use of a very linear multislope charge balance integrator and a custom VLSI IC. The digitization process starts with a Command Register update via the parallel interface. Following a 10 µs delay to allow for multiplexer settling time, the input signal is integrated for

Time Tint. During this time, packets of energy are periodically removed. This architecture keeps the integrator output "ratcheting" around the input voltage, helping to optimize this circuit for linearity, low noise, and speed. After this time, the input signal is disconnected and a reference integration follows for approximately 5 ms. During both integration cycles, a 26-bit counter keeps track of the accumulated charge due to the input signal. The counter's output is then latched into the Data Registers. It remains latched until a subsequent digitization. This is shown in Figure 9 as a LOW to HIGH transition of $\overline{WR}$.

ADC5042 Output Data Format

The output data registers are updated with the contents of a 26-bit counter, which keeps track of the input signal charge accumulated during the digitization process. This data will contain a span and offset error, which is easily removed by the host microprocessor.

The span is defined as the difference between the counts due to a minus full scale input (–5V) and the counts due to a plus full scale input (+5V). Note that for the ADC5042, a –5V input produces the most counts and a +5V signal produces the least counts. The ideal span is normally 2n where n = the resolution selected; however, the actual span in the ADC5042 will be greater than the ideal span. This span error actually results in a slight increase in resolution and need only be calibrated out. It has no other effect on the resulting data.

The offset error is due to an offset voltage added to the input signal during signal integration. This offset has the effect of producing a larger number of counts for a given input than would normally be expected (this is why a 26-bit counter is necessary even though the maximum resolution is 24 bits). Since it is a true offset, these additional counts are constant for any given input signal and thus contribute no gain error. They are simply subtracted from the final result with the host microprocessor.

Calibration of ADC5042 Output Data

Calibration of the output data to eliminate the above-mentioned offset and span errors is very simple. The offset counts are quantified by digitizing a 0 volt input. This can be either the ADC5042's Offset Channel or any other multiplexer channel connected to signal ground. The span error is measured by digitizing a known voltage near either plus or minus full scale. This can be either the ADC5042's Reference Channel or a stable input on any other multiplexer channel. Using a calibration algorithm contained in the host microprocessor, such as the one shown in Figure 10, the resulting output data is converted to volts and its absolute accuracy follows the reference used.

A useful variation of calibrating the ADC5042 utilizes two references that can be used for the span reading, one at –FS and one at + FS (where Vref = [+FS] - [–FS]). This has the advantage of correcting over the full dynamic range, but requires two multiplexer channels devoted to a reference.

Since the span and offset errors of the ADC5042 are time- and temperature-sensitive, calibration should be done on a periodic basis.

$$V_{OUT}\text{ (volts)} = (V_{IN}\text{ COUNTS-OFFSET COUNTS}) * \frac{V_{REF}\text{ (volts)}}{\text{(REF COUNTS-OFFSET COUNTS)}}$$

Figure 10. Calibration Formula.

The frequency of calibration is application-specific and should be based on the stability of the operating environment and resolution selected. However, it should always be done at power-up and at every conversion until the ambient operating conditions have stabilized.

The calibration should be done periodically to remove errors associated with a change in the ambient temperature or time. The optimum frequency is determined by system characteristics and operating environment.

A 1°C change in temperature represents a worst-case 30 ppm (combined offset and gain TC) change or two LSBs at 16 bits.

To maintain an absolution accuracy TC of ±1 LSB, calibration is required for every 0.5°C change in ambient temperature. Should the converter not be calibrated every 0.5°C change, errors as high as 15 ppm will result.

ADC5042 Pin Assignment

PIN #	FUNCTION	DESCRIPTION
1	X1/CLKIN	3.072 MHz Clock/Crystal Input
2	X2/CLKOUT	3.072 MHz Crystal Input
3	$\overline{WR}$	Active Low Input Used with $\overline{CS}$ for Write Operations
4	$\overline{RD}$	Active Low Input Used with $\overline{CS}$ for Read Operations
5	$\overline{CS}$	Active Low Input Used with $\overline{RD}$ and $\overline{WR}$
6	A0	Active High Input Used to Select Data Registers
7	A1	Active High Input Used to Select Data Registers
8	+VA	+11.5 to 15.75 Volt Input
9	–VA	-11.5 to -15.75 Volt Input
10	AGND	Analog Ground
11	AMP OUT	Output of Internal Amplifier
12	AMP+	Non-Inverting Input of Internal Amplifier
13	AMP-	Inverting Input of Input Amplifier
14	SIG GND	Signal Ground
15	CH1	Multiplexer Input Channel 1
16	CH2	Multiplexer Input Channel 2
17	CH3	Multiplexer Input Channel 3
18	CH4	Multiplexer Input Channel 4
19	CH5	Multiplexer Input Channel 5
20	CH6	Multiplexer Input Channel 6
21	REF IN	5.0 Volt Reference Input
22	REF OUT	Internal 5.0 Volt Reference Out
23	MUX OUT	Internal Multiplexer Output
24	MA0	Active High Internal Multiplexer Address Output
25	MA1	Active High Internal Multiplexer Address Output
26	MA2	Active High Internal Multiplexer Address Output
27	MXEN	Active High Internal Multiplexer Enable Output
28	BUSY	Active High Output Indicates Digitization Active
29	$\overline{RESET}$	Active Low Input Resets All Logic
30	50/$\overline{60}$ SELECT	Active Low Selects 60 Hz Integration Line Cycles
31	DGND	Digital Ground
32	+VD	+5 Volts
33	D0 (LSB)	Bi-Directional Data Bit
34	D1	Bi-Directional Data Bit
35	D2	Bi-Directional Data Bit
36	D3	Bi-Directional Data Bit
37	D4	Bi-Directional Data Bit
38	D5	Bi-Directional Data Bit
39	D6	Bi-Directional Data Bit
40	D7 (MSB)	Bi-Directional Data Bit

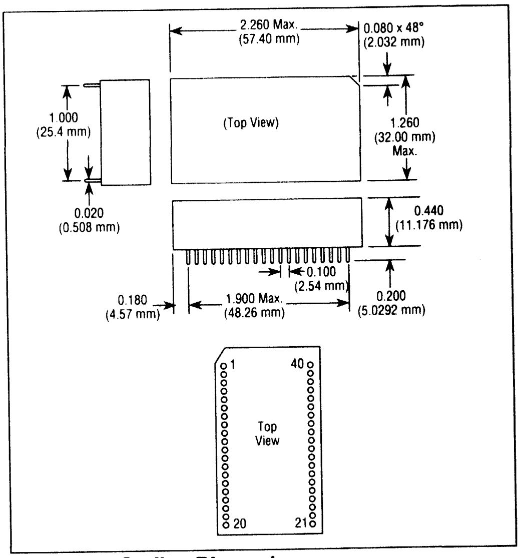


Figure 11. Outline Dimensions.

Ordering Guide

Specify:

ADC5041 – Full UART Interfacing

ADC5042 – µP Interfacing

High Precision, High Speed, 17-Bit Integrating A/D Converter

In a Hybrid, 40-pin Dual-In-Line Package

Introduction

The AH30217 is an ultra-high-resolution 17-bit integrating A/D converter in a hybrid, 40-pin, dual-in-line package. Performing up to 300 conversions per second, the AH30217 ensures accurate conversions by effectively eliminating internal drifts using a four-phase triple-slope integrating conversion scheme and an autozero before each conversion. The AH30217 features TTL-compatible data and controls, making it easy to integrate into a system. Furthermore, the hybrid package minimizes the amount of valuable printed circuit board real estate required to deliver this level of performance.

The AH30217 is particularly suited for high precision data acquisition and control systems used in industrial process control. In such harsh environments, data conversion is plagued by many problems, including common modé voltages and ground-loops. However, the differential inputs and autozero of the AH30217 eliminate these and similar problems, freeing users from having to locate millivolt level errors in their systems. Furthermore, the AH30217 has an absolute accuracy adjustable to within ±0.0025% FSR, a differential linearity of ±0.2 ppm FSR, and a relative accuracy of ±7.5 ppm FSR, assuring meaningful 17-bit information. The AH30217 is the A/D converter of choice for high resolution industrial data acquisition systems.

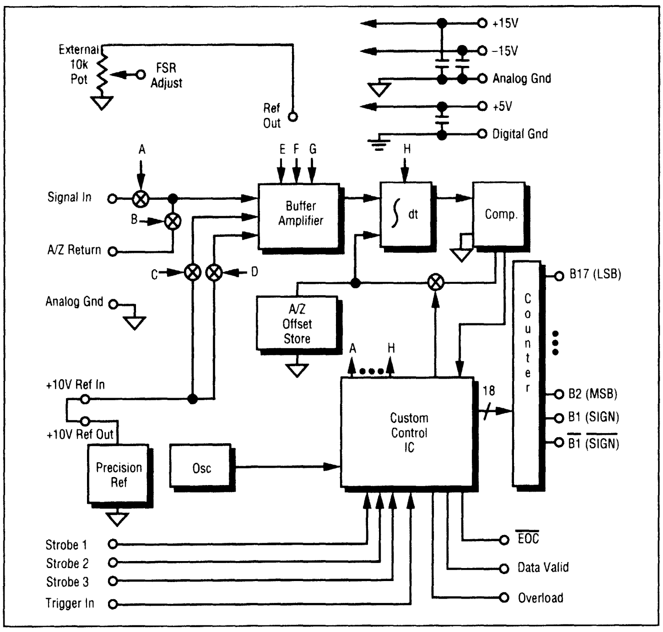


Figure 1. The AH30217 Block Diagram

Features

- ❑ Ultra-High Resolution (17 Bits)
- ❑ High Speed (300 Conversions/Second)
- ❑ Hybrid 40-pin DIP
- ❑ High Input Impedance (1000 MΩ)
- ❑ Excellent Differential Linearity (±0.2 ppm FSR)
- ❑ Autozero Before Each Conversion
- ❑ High Absolute Accuracy (±0.0025% FSR)
- ❑ Low Input Current (50 nA @ 100 Conversions/Second)
- ❑ TTL Compatibility
- ❑ Low Power (600 mW)
- ❑ Ratiometric Measurements Using External Reference
- ❑ External System Offset Compensation

Applications

- ❑ High Resolution Data Acquisition and Control Systems
- ❑ Precision Chemical Process Control Systems
- ❑ Gas Chromatography
- ❑ High Resolution Laboratory and R&D Systems
- ❑ Analytical Instrumentation
- ❑ High Precision Automatic Test Equipment
- ❑ Precision Pharmaceutical Mixing and Grading Systems

ANALOGIC®
The World Resource for Precision Signal Technology

AH30217

Specifications [1]

ANALOG INPUT

Input Configuration
Differential (see Figure 5) (2)

Input Range
±10V (±15V without damage) (3)

Input Impedance
1000 MΩ Min., 50 pF Max.

Input Current
50 nA @ 100 conversions/second

DIGITAL INPUTS

Logic Levels
Logic "0"
0.8V Max.

Logic "1"
2.0V Min.

Trigger Pulse Width (4)
0.1 µs Min., Negative edge starts conversion

Control Inputs
STROBE 1
Active Low, Strobes B10-B17

STROBE 2
Active Low, Strobes B2-B9

STROBE 3
Active Low, Strobes B1 and $\overline{\text{B1}}$

DIGITAL OUTPUTS

Data Outputs
16 data bits, SIGN (B1), $\overline{\text{SIGN}}$ ($\overline{\text{B1}}$)

Fan-Out
2 LSTTL Loads Max.

Output Coding
Sign Magnitude (5)

Output Voltage
Logic "0"
0.4V Max.

Logic "1"
2.4V Min.

$\overline{\text{EOC}}$
Active Low

Data Valid
Active High

Overload
Active High

DYNAMIC CHARACTERISTICS

Conversion Rate
0-300 conversions/second, controlled by external command

Signal Integration Time
512 µs

Conversion Technique
4-phase, triple-slope integrating analog-to-digital conversion, autozeroed before each conversion

TRANSFER CHARACTERISTICS

Resolution
16 bits plus sign

Relative Accuracy
±12 ppm FSR Max.

Differential Linearity
±0.2 ppm FSR (±3σ)

Noise
10 µV RMS Max.

Absolute Accuracy
±0.005% FSR, without adjustment;
±0.0025% FSR Max., adjusted

STABILITY (0°C TO 70°C)

Offset Voltage
±3 µV/°C Max.

Gain
±6 ppm/°C Max.

Supply Rejection
Offset
15 ppm/% Max.

Gain
15 ppm/% Max.

Warm-Up Time
5 Min.

POWER REQUIREMENTS (6)

Supply Range
±15V Supplies
14.5V Min., 15.5V Max.

+5V Supply
4.75V Min., 5.25V Max.

+15V Current Drain
20 mA

–15V Current Drain
16 mA

+5V Current Drain
10 mA

Power Consumption
600 mW

ENVIRONMENTAL & MECHANICAL

Temperature Range
Rated Performance
0°C to 70°C

Storage
–25°C to +85°C

Relative Humidity
0 to 95% non-condensing up to 70°C

Dimensions
1.1" x 2.2" x 0.3", 40-pin triple DIP

SPECIAL FEATURES

Ratiometric Measurements
+10V ±10% external reference may be used in place of internal reference and connected to REF IN

External System Offset Compensation
±10 mV Max., may be compensated. Connect to A/Z RTN.

NOTES:

1. All specifications guaranteed at 25°C unless otherwise noted. Supplies are ±15V and +5V.
2. Maximum common mode voltage input is ±10 mV.
3. Other input ranges are available. Consult factory.
4. Trigger is locked out when the conversion starts until the end of conversion.
5. Consult factory for other output coding.
6. Analogic highly recommends the use of linear power supplies with its high performance, high resolution A/D converters. However, if system requirements provide only a +5V supply and limited space, the use of the Analogic SP7015 DC-to-DC converter will provide a low noise solution which will not degrade the AH30217 performance.

Specifications subject to change without notice.

Principles of Operation

The innovative quadraphasic design of the AH30217 completes a conversion in four phases. This technique is depicted in Figures 1 and 2. The four phases are: the autozeroing (AZ); signal integration (∫x); integration of ref high (∫ ref hi); and integration of ref low (∫ ref lo). Timing signals for each of the phases are coordinated in a custom IC in response to various digital and analog input signals. When not in a conversion mode, the converter is placed automatically into its autozero phase. The autozero phase of the unit is considered part of the conversion time and is included in the time when $\overline{EOC}$ is high. The function of the autozero time is to ensure that the memory capacitor is charged to compensate for any internal drifts and any external offsets introduced at the module pin connections.

The falling edge of trigger causes the timing counters (internal to the custom IC) to be reset to zero. At this time the analog circuitry is changed from autozero to integrating the unknown input voltage. Subsequent triggers are locked out. The input signal (and any stored AZ offset) is integrated for a period of approximately 512 µs.

Program control then shifts the unit into Phase 2, where the input signal is replaced by a high current, opposite polarity reference. This discharges the integrating capacitor at a high rate as shown in Figure 2. During this phase, the output counters are incremented beginning with B9 counting up to B1 (MSB).

When the integrating capacitor has been discharged to a preset level, the program control begins Phase 3. The high current reference is replaced by a low current reference, and the low bit counters beginning with B16 (LSB) are incremented. This phase continues until the integrating capacitor is discharged to its initial value.

The unit is then set to the Phase Zero mode. After a fixed time which allows the autozero loop to stabilize, the $\overline{EOC}$ is brought low ending the conversion. At this time the output data is valid and remains valid until the end of the next conversion. Appropriate delays are introduced between phases to eliminate conversion errors which could result from the settling of the program-switching circuits.

The sign magnitude data word is tri-stated by means of three strobe inputs, allowing the AH30217 to interface to an 8-bit microprocessor bus. Strobe 1 enables B10-B17; Strobe 2 enables B2-B9; Strobe 3 enables B1 and $\overline{B1}$.

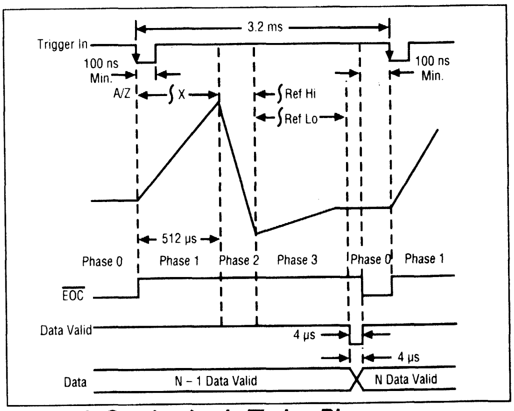


Figure 2. Quadraphasic Timing Diagram.

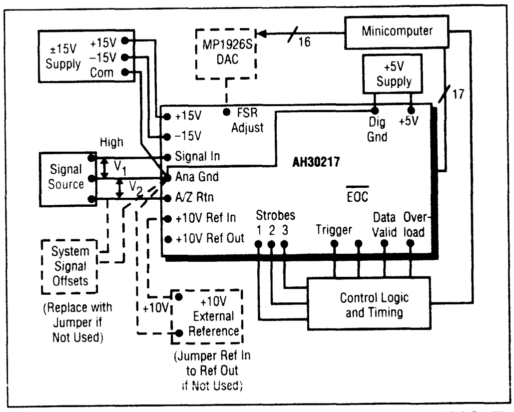


Figure 3. Connecting Power & Signals to AH30217.

Using the AH30217

As shown in Figure 3, the AH30217 is connected to the signal source, a trigger command, three sources of power (+5 VDC and ±15 VDC), and an optional external reference. The second signal input may be used to remove common mode voltages or to introduce corrections to the input signal to compensate for other system errors. Note that the rising edge of Data Valid can be used to latch the data from the AH30217. The optional digital-to-analog converter is used to calibrate +FS and –FS as described below; a potentiometer can be used instead.

The Overload pin goes high when the input voltage exceeds the full scale range of the A/D converter. This occurs beyond the ±10V input range of the AH30217.

Output Coding and Trim Procedure

Figure 4 shows the output coding of the AH30217 A/D converter. The coding format is sign magnitude. The AH30217 can be calibrated using an external potentiometer connected to FSR Adjust as shown in Figure 1 or using a digital-to-analog converter connected to FSR Adjust as shown in Figure 3.

The example below demonstrates the trim procedure. Measure the voltage required to obtain a reading of 11111111111111111/0 (where the LSB is alternating equally between 0 and 1). Measure the voltage required to obtain a reading of 01111111111111111/0. Add the two voltages together and divide the sum by two. Add this voltage to the ideal positive and negative full scale voltages — 1/2 LSB (±9.999847V – 0.000076V = ±9.999771V), and use one of these voltages as the input voltage. The appropriate digital code (11111111111111111/0 or 01111111111111111/0) should be obtained by varying the FSR Adjust potentiometer.

Example of Trim Procedure:

11111111111111111/0	+9.999420V
01111111111111111/0	–0.000530V
	–0.000110V
–0.000110V ÷ 2 =	–0.000055V
±9.999847V – 0.000076V =	±9.999771V
+9.999771V – 0.000055V =	+9.999716V
–9.999771V – 0.000055V =	–9.999826V
11111111111111111/0	+9.999716V
01111111111111111/0	–9.999826V

Truth Table

Input Voltage	**Digital Outputs**		
Sign Magnitude	Sign	MSB	LSB
+9.999847V	1	1111111111111111	
0.000000V	1	0000000000000000	
–9.999847V	0	1111111111111111	

Figure 4. AH30217 Output Coding.

Input Connections to the AH30217

Input Signals: The AH30217 encodes the difference between two input signals (Figure 5). By providing a differential input, the AH30217 eliminates small system ground-loop voltages (up to 10 mV), common mode voltages, and minor system offsets. Use the 3-wire input configuration as illustrated in Figure 5.

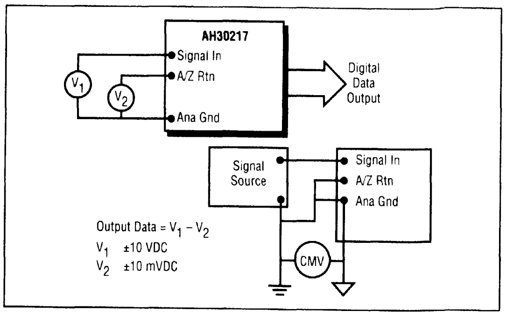


Figure 5. Connecting Input Signals to Remove CMV.

Reference: True ratiometric measurements may be made with the AH30217 by replacing the internal reference with a 10 VDC external reference. Remove the jumper between pin terminals REF OUT and REF IN and connect +10 VDC ±10% between REF IN and ANA RTN.

Typical Application

The AH30217, when connected as shown in Figure 7, provides wide dynamic range. In this application the output of a Gas Chromatograph is connected to a programmable gain amplifier (PGA). The output of the PGA is input to the AH30217, and the selected gain is indicated by three output bits from the PGA.

Once the gain has been properly set and sufficient time has been allotted after $\overline{EOC}$ for autozero, the control logic issues a convert command to the AH30217. When the $\overline{EOC}$ signal is obtained, valid 20-bit data digitizing a 21-bit input dynamic range is available at the output. In this system the AH30217 A/Z RTN is jumpered to Analog GND, and any common mode voltage between source, system, and measuring system grounds is rejected in the PGA.

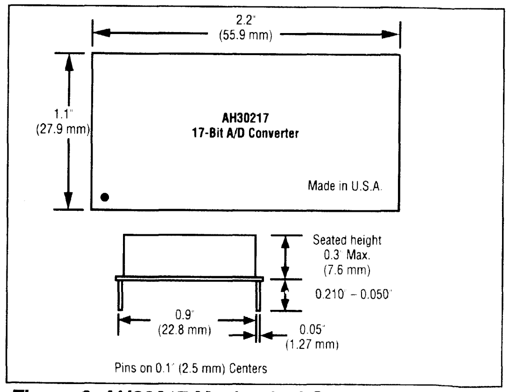


Figure 6. AH30217 Mechanical Outline.

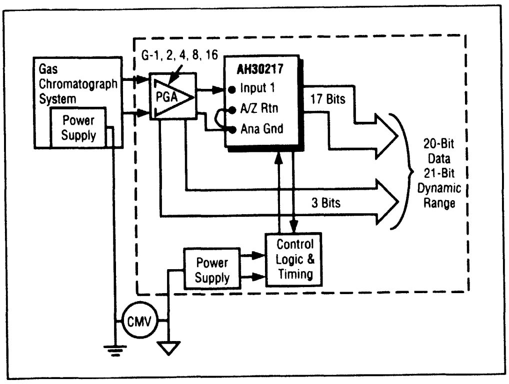


Figure 7. Typical AH30217 Application.

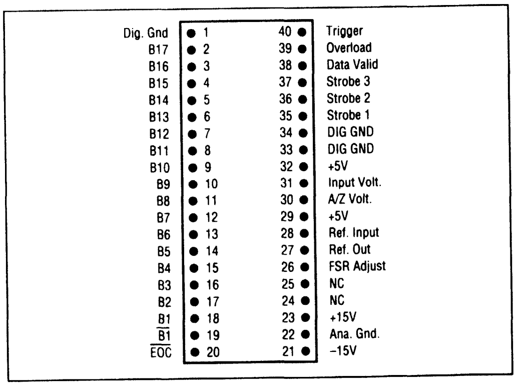


Figure 8. AH30217 Pinout.

Ordering Guide

17-Bit Integrating A/D Converter
Specify **AH30217P Plastic Package**
Specify **AH30217C Ceramic Package**

DC to DC Converter
Specify **SP7015**

For full scale ranges other than ±10V, or for output coding other than sign magnitude, or for signal integration times other than 512 µs, or for conversion rates greater than 300 per second, consult factory.

MP2316A

16-Bit Floating Input, Programmable Gain, Analog Processor

Providing Very High Isolation

Introduction

The MP2316A is a floating input, programmable gain analog converter-processor front end. It provides very high isolation between high resolution digital systems and large numbers of multiplexed analog input signals, especially in high common-mode voltage industrial environments such as process control, data acquisition systems and HVAC systems.

The MP2316A consists of an input stage, a 13-gain programmable gain amplifier, a buffered dual-slope integrating A/D, a precision reference, an isolated DC/DC converter, and all the circuits required to complete the analog portion of a precision, 16-bit data acquisition system. The entire interface to the digital host system is through three transformer-isolated lines; two inputs for control and one output line for conversion results, which are in the form of an elapsed time between a pulse on one control line and the End-of-Conversion (EOC) signal from the converter.

The high isolation of the analog inputs from the digital output is achieved by an intrinsic CMRR of 90 dB due to high quality magnetic isolators, an overall CMRR of 150 dB, a 60 dB line frequency normal mode rejection ratio, and up to ±500V (AC peak and DC) of common mode isolation.

Continued on page 93.

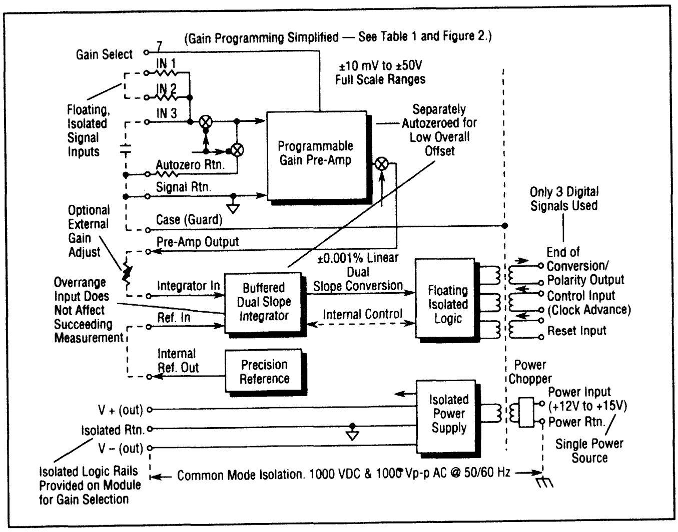
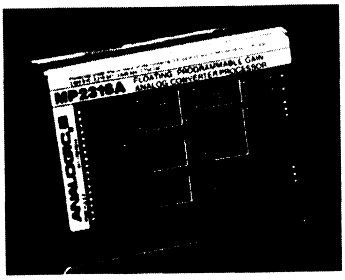


Figure 1. MP2316A Functional Block Diagram.



Features

- ❑ Programmable Gain Amplifier Provides 13 Switch Selectable Full Scale Ranges from ±10 mV to ±50V
- ❑ Floating Isolated Input Provides 500V Isolation from Signal Common to Output Common
- ❑ 150 dB Common Mode Rejection Ratio
- ❑ Guarded Input Allows Multiplexing of Input Lead Shields
- ❑ Time Interval Output Proportional to Input Voltage
- ❑ ±0.001% FSR Linearity Consistent Performance with 16-Bit Resolution
- ❑ Isolated Output Voltages Provides Power for Sensors
- ❑ High Stability; 0.3 µV/°C Offset, 12 ppm/°C Range
- ❑ Flexible Power Supply Requirement +12V to +15V
- ❑ Small Size – 2" x 3" x 0.51"

Applications

- ❑ Industrial Process Control
- ❑ Heating, Ventilating and Air Conditioning (HVAC)
- ❑ Thermocouple Measurement
- ❑ Bridge Measurement
- ❑ Data Acquisition Systems

ANALOGIC®
The World Resource for Precision Signal Technology

MP2316A

Specifications[1]

ANALOG INPUT

Configuration
Floating, isolated, three wire

Full Scale Range (FSR)
Selectable ranges from ±10 mV to ±50V (See Table 1)

Maximum Common Mode Voltage
±500 VDC or AC peak, (SIGNAL RETURN to POWER RETURN) [2]

Common Mode Rejection Ratio
150 dB minimum at 50 or 60 Hz, with integration period within ±0.05% of the power line frequency

Input Impedance
FSR ≤ ±5V – 100 MΩ minimum
FSR > ±5V – 1 MΩ nominal

Bias Current
300 pA, typical [3]

Maximum Input
264 VAC RMS continuous without damage [2,4]

ISOLATED VOLTAGE OUTPUTS

Output Voltage
+8V nominal (V+); –10V nominal (V–); the amount of current drawn from V+ must never exceed that drawn from V– by more than 3 mA; the total current drawn from both outputs must not exceed 6 mA.

ACCURACY

Output Coding
Time interval proportional to the magnitude of the input voltage, plus sign decision based on polarity of input

Resolution
Depends on count rate of external counter; up to 16 bits (15 magnitude bits plus sign bit) achievable with appropriate external logic

Transfer Accuracy
Consistent with 15-bit resolution, with external calibration adjustment

Differential Non-linearity
±0.001% FSR, typical

Integral Non-linearity
±0.006% FSR, typical

Offset
RTI – Externally adjustable to zero [5]
RTO – ±15 ppm FSR, maximum [6]

Noise
3 µV RMS or 10 ppm FSR RMS maximum, whichever is greater; assumes a 1.5 µF capacitor (Cx) across IN3 and SIGNAL RETURN per Figure 2

STABILITY

Range Tempco (0°C to 70°C)

FSR ≤ ±5V
±12 ppm FSR/°C typical,
±25 ppm FSR/°C maximum

FSR > ±5V
±20 ppm FSR/°C typical,
±30 ppm FSR/°C maximum

RTI Offset Tempco (0°C to 70°C)
±0.3 µV/°C typical

Power Supply Rejection Ratio
±0.002% FSR/percent power supply change

Recommended Recalibration Intervals
6 months

DYNAMIC PERFORMANCE

Input Integration Time (Phase 1)
1/60 second ±0.05% when synchronized to 60 Hz power line; 1/50 second ±0.05% when synchronized to 50 Hz power line [7]

Full Scale Reference Integration Time (Phase 2)
One-half the input integration time, nominal

Integrator Autozero Time (Phase 3)
1.9 µs, minimum, no maximum limit

Time to recover from Overrange Input
1.9 µs [8]

Overall Throughput Rate
Up to 37 measurements/second when synchronized to 60 Hz line; Up to 31 measurements/second when synchronized to 50 Hz line

DIGITAL INPUT/OUTPUT

(See Figure 7)

Input Lines
12V CMOS compatible; negative pulses

Reset Line
A negative pulse on this line initiates the autozero phase; low level is active;
200 ns pulse width minimum, 3 µs maximum [9]

Clock Advance Line (See Figure 6)
Negative-going (leading) edge is active; each pulse must be low for 100 ns minimum

First Pulse (Φ1)
Initiates input integration

Second Pulse (Φ2)
Strobes out the Polarity (decision) Pulse

Third Pulse (Φ3)
Initiates reference integration

Output Line
12V CMOS-compatible, positive pulses; positive-going (leading) edge is active; 100 ns minimum pulse width, 4 µs maximum; 100 ns rise and fall times, typical

Polarity Pulse
Occurrence of an output pulse upon receipt of the polarity strobe (Φ2) indicates that the input signal has a negative polarity; absence of a pulse at this time indicates positive polarity

End-of-Conversion (EOC) Pulse
The elapsed time from the start of reference integration until EOC occurs is directly proportional to the magnitude of the input signal plus a constant 1 µs, nominal, delay

POWER SUPPLY REQUIREMENTS

+12V to +15V
80 mA typical, 125 mA maximum

ENVIRONMENTAL & MECHANICAL

Operating Temperature Range
0°C to +70°C

Storage Temperature Range
–25°C to +85°C

Relative Humidity
0 to 80%, non-condensing to 40°C

Dimensions
2.0" x 3.0" x 0.51"
(50.8 x 76.2 x 12.9 mm)

Shielding
Electrostatic 6 sides, Electromagnetic 5 sides

Case Potential
At the GUARD potential (equals common mode potential referenced to POWER RETURN)

NOTES:

1. Assumes a 1 kΩ gain adjust potentiometer is connected per Figure 1.
2. With Cx = 1.5 μF installed between AUTOZERO RETURN and IN3, or with external diode input protection circuit per Figure 2.
3. 500 pA maximum at 40°C; doubles every 10°C above 40°C.
4. Input 1 to SIGNAL RETURN; INPUT 2 to SIGNAL RETURN.
5. ±50 μV maximum, externally adjustable to zero via AUTOZERO RETURN (See Autozero Connection Section).
6. Externally adjustable via 1 μs nominal delay between Clock Advance Φ3 and start of user's counter.
7. Sign decision is made immediately prior to completion of the input integration phase.
8. Assumes that Reset is issued whenever EOC does not occur within the nominal full scale integration time.
9. Measured between 50% points.

All specifications guaranteed at 25°C unless otherwise noted. Specifications subject to change without notice.

Continued from page 91.

The programmable gain amplifier (PGA) provides a simple and flexible scheme for selecting a ±10 mV to ±50V full scale range while maintaining full isolation. Gain may be changed by applying the MP2316A's own isolated auxiliary voltage outputs, via switches, to the gain programming pins (see GAIN PROGRAMMING). An autozero return from the PGA allows long-term system offset drifts to be essentially eliminated. Both the PGA and the integrator are autozeroed between conversions, so that DC offset is less than 50 μV RTI (adjustable to zero).

By fully implementing the most difficult (analog) functions, the MP2316A is an ideal starting point for designing a wide variety of low speed, precision data acquisition systems. By parallel connection of multiple units, higher throughputs can be achieved.

USING THE MP2316A

Gain Programming

The three gain stages shown in Figure 2 allow selecting any of the 13 gains from 0.05 to 250 inclusive, providing full scale ranges from ±50V to ±10 mV. The external potentiometer connections shown allow fine adjustment of any selected range. For example, a 1 kΩ pot provides a ±4.5% adjustment, more than adequate for obtaining either a ±1.000V FSR or a ±1.024V FSR with one basic gain selection.

Each of the gain stages may be externally configured using either switches, relays, or opto-isolators, or by any other convenient means available in the host system. The module's own floating output voltages may be used for controlling the MP2316A's internal solid-state switches, A through H, per the inset of Figure 2.

External gain and offset adjustment potentiometers, if used, can be switched similarly. It is possible, then, to configure and trim the MP2316A to provide nearly any desired full scale range(s) and/or any desired range-to-range absolute accuracy, while maintaining full isolation. When the maximum attainable accuracy is require, it is recommended that each range be calibrated individually.

Table 1. MP2316A Range Programming

	Gain Select Pin Connections [2]							
FSR [1]	**A**	**B**	**C**	**D**	**E**	**F**	**H**	**G1** [3]
±10 mV	1	0	0	0	0	0	1	1
±20 mV	0	1	0	0	0	0	1	1
±50 mV	1	0	0	0	0	1	0	1
±100 mV	1	0	0	0	1	0	0	1
±200 mV	0	1	0	0	1	0	0	1
±1V	1	0	0	1	0	0	0	1
±2V	0	1	0	1	0	0	0	1
±2.5V	1	0	1	0	0	0	0	1
±5V	0	1	1	0	0	0	0	1
±10V	1	0	0	1	0	0	0	0.1
±20V	0	1	0	1	0	0	0	0.1
±25V	1	0	1	0	0	0	0	0.1
±50V	0	1	1	0	0	0	0	0.1

Notes to Table 1.

1. Full scale ranges (FSRs) specified with 500Ω nominal between gain adjust terminals @ 25°C ±5°C. A resistance change of 0 to 1 kΩ between gain adjust terminals results in a nominal gain change of 9%.
2. "0" denotes this pin connected to the V– isolated output; "1" denotes this pin connected to the V+ isolated output through a resistor.
3. Input Gain (see Figure 2 and Input Connections).

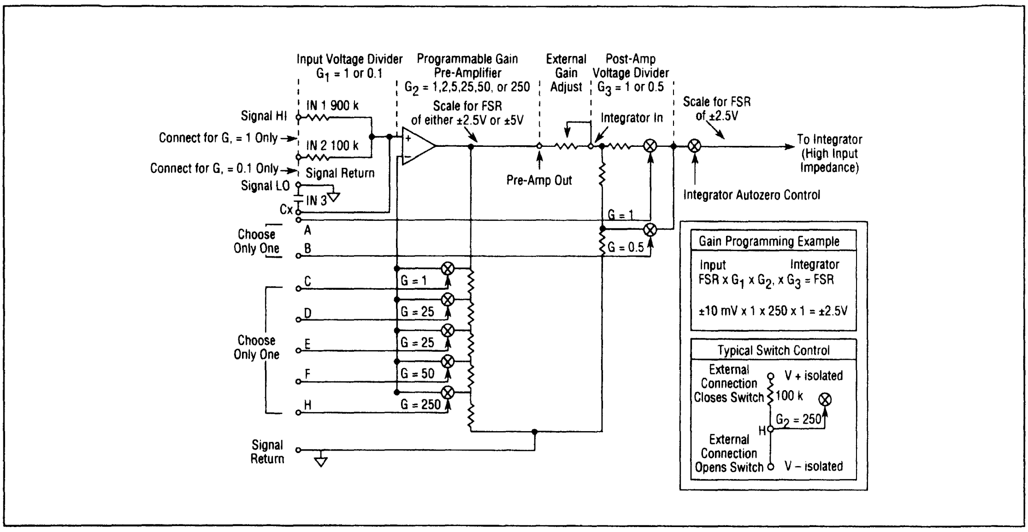


Figure 2. MP2316A Gain Programming.

INPUT CONSIDERATIONS

Input Connections

For full scale ranges larger than ±5V, the analog input signal is connected to IN1, and IN2 is externally connected to SIGNAL RETURN. In this configuration, the input stage's gain of 0.1 allows use with input signals having full scale ranges up to ±50V.

For full scale ranges nominally ≤ ±5V, the analog input signal is connected to IN2, which provides unity gain. IN1 should be tied to IN2 to prevent noise pick up. By connecting a 1.5 μF capacitor between IN3 and ground, high frequency noise filtering on any range can be accomplished. The low-pass filter thus formed (RC = 900 kΩ/1.5 μF for IN1 and RC = 100 kΩ/1.5 μF for IN2) will reduce the usable input signal bandwidth.

Case Potential

The Case (GUARD) pin may be tied to SIGNAL RETURN as shown in Figure 1, and/or to the lead shield, if one is used. If lead shields for different channels carry different potentials in the system, and the shields, are not multiplexed to the Case pin, it is recommended that each shield be tied to local earth at its sensor, while the Case pin is tied to SIGNAL RETURN. Optimum system performance will generally be obtained by using twisted shielded pair for each channel.

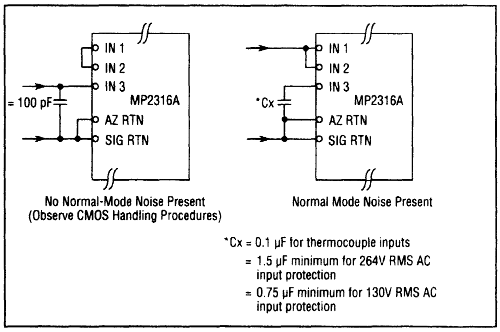


Figure 3. Input Configurations.

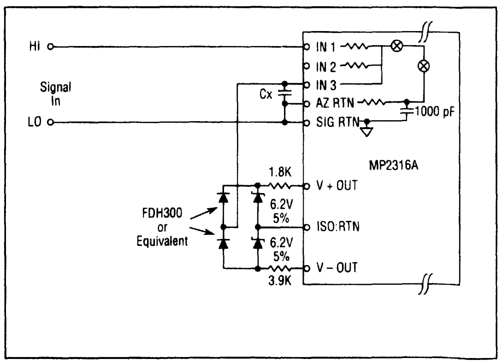


Figure 4. Diode Input Protection Circuit.

Input Overvoltage

The specifications call out a maximum continuous input without damage of 264 VAC RMS. This assumes a value for Cx of 1.5 μF connected between the IN3 and SIGNAL LO pins as shown in Figure 2. Failure to use this capacitor will result in damage to the unit under the specified input conditions. It should be noted that this capacitor will form a low-pass filter on the input (RC = 900 kΩ/1.5 μF for INPUT 1 and RC = 100 kΩ/1.5 μF for INPUT 2). This will reduce the usable signal bandwidth at the input to the A/D.

Noise

The specification for noise performance assumes a value of 1.5 μF for Cx. If the capacitor is not used to low-pass filter the input, noise in excess of the specification can occur.

The input configuration can be modified depending on whether or not normal mode noise is present. See Figure 3.

Thermocouple Inputs

When used with thermocouple inputs, the value of Cx between IN3 and SIGNAL LO should be ≥0.1 μF to limit the input response to approximately 12 Hz.

Input Protection

It is recommended that the diode input protection circuit in Figure 4 be used to protect the MP2316A from large common mode and normal mode spikes, such as those that occur when relay contacts are switching signal sources to the MP2316A input.

Autozero Connection

Using the AUTOZERO RETURN, offsets that may occur between the SIGNAL RETURN and the common of the sensor subsystem (see Figure 5) can essentially be eliminated. The maximum offset that can be eliminated is 20% of the selected full scale range if the input voltage divider gain is set at unity. For larger full scale ranges where the input divider is set at 0.1, the maximum offset eliminated is 2% of the full scale range. A small signal potentiometer installed between SIGNAL RETURN and AUTOZERO RETURN can be used to zero the MP2316A's small (±50 μV RTI maximum) offset, per Figure 5.

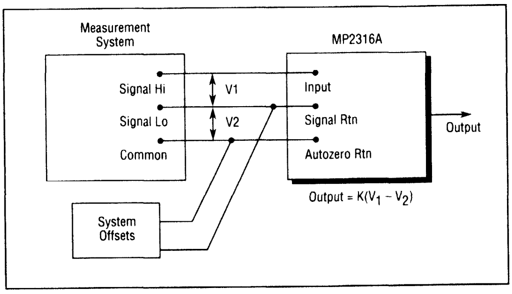


Figure 5. The MP2316A's Three-Wire Input Configuration Essentially Eliminates Long Term Sensor System Offsets.

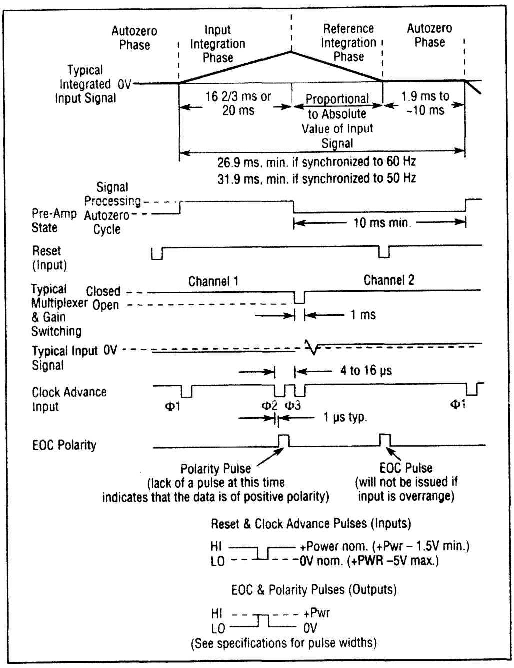


Figure 6. MP2316A Timing Diagram.

Table 2. Reference Integration Time (Linear).

	Line Frequency	
Input	60 Hz	50 Hz
−Full Scale	8.333 ms	10.000 ms
0V	0.001 ms	0.001 ms
+Full Scale	8.333 ms	10.000 ms

Isolated Output Voltages

The MP2316A is provided with isolated voltage outputs of +8V and −10V nominal. These can be used to power strain gauges, or other sensors. It is important to limit the total current drawn from both outputs to 6 mA or less, and to ensure that the amount of current drawn from the V+ output never exceeds that drawn from the V− output by more than 3 mA.

Reference Connections

The MP2316A contains its own isolated precision reference source (–4.75V). This reference is brought out as a test point (INTERNAL REFERENCE OUT), and should be jumpered to REFERENCE IN for most applications.

For true ratiometric applications, a floating external supply that excites the system's sensors may also be applied, via a buffer, to REFERENCE IN (while INTERNAL REFERENCE OUT floats). If used, such a reference should be –4.75V ±10%.

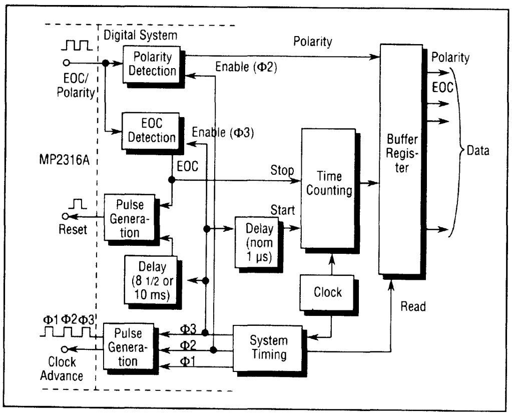


Figure 7. Applications Diagram — Functional Block Diagram of MP2316A External Control Logic, Implementable in Either Hardware/Software.

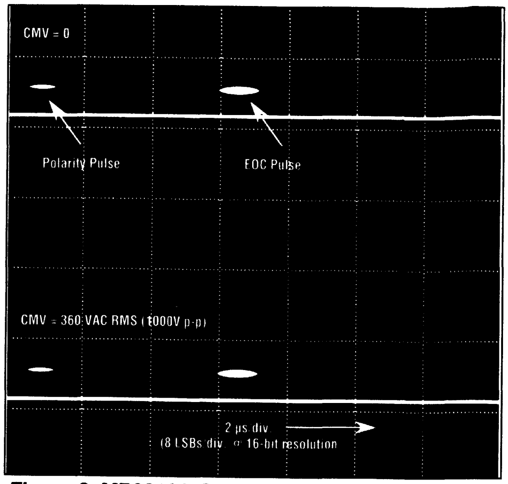


Figure 8. MP2316A Common Mode Rejection Ratio Test (360V RMS CMV, 37 Hz Measurement Rate, ±50 mV FSR).
Note: Pulse polarity inverted for display only.

The upper trace shows the Polarity and EOC pulses for a zero volt input with no common mode voltage present. The lower trace shows the same pulses when 360V RMS of CMV is present, also with a zero volt input signal. A time exposure is used to display both conversion results. In the lower trace, EOC occurs 0.5 µs later than in the upper trace. At 16-bit resolution, this shift is equivalent to 2 LSBs, or only 3 µV common mode error — on a full scale range of ±50 mV — resulting from 360V RMS CMV. Thus the CMRR measured is greater than 160 dB, 10 dB better than the MP2316A specification!

Timing and Control

The Timing Diagram (see Figure 6) shows the operation of a multiplexed data acquisition system that uses the MP2316A; the Applications Diagram (Figure 7) indicates the corresponding external logic functions. These functions can be implemented via either hardware or software, depending on the economics of the host digital system. The operational timing contains three phases summarized as follows:

1. Integrate the input signal
2. Integrate the precision reference for a maximum of one-half of the input integration time
3. Autozero the integrator

A description of operation during each of these phases follows, starting with the autozero phase.

Autozero Phase

Each measurement cycle begins with a pulse on the RESET line, which initiates autozeroing of the precision integrator. A minimum of 1.9 ms should be allowed for autozeroing. If the MP2316A input is overranged, the autozero circuit will ensure recovery within this time.

Input Integration Phase

When the first pulse (Φ1) is received on the CLOCK ADVANCE line, the autozero cycle terminates and integration of the input signal begins.

The second pulse on the CLOCK ADVANCE line (Φ2) strobes out the results of a polarity test that the module performs on the input signal during the integration. This second pulse should occur from 10 µs before the end of this signal integration period. If the input signal is negative, the MP2316A issues a pulse on the EOC/POLARITY line nominally within 1 µs of receipt of the Φ2 pulse. If the input signal is positive, the MP2316A issues no pulse on the EOC/POLARITY line at this time.

Reference Integration Phase

The third pulse is applied to the CLOCK ADVANCE (Φ3) from 4-16 µs after the Φ2 pulse, at which time the module automatically switches the integrator's input to the precision reference, and the preamplifier's input to the AUTOZERO RETURN line. Because the preamplifier is disconnected from the integrator, any gain and/or multiplexer switching needed for the next measurement may be made during this phase without affecting the accuracy of the reference integration.

Within nominally 1 µs after receiving Φ3, the MP2316A begins discharging the integration capacitor via a precision reference of opposite polarity from that of the input signal. If the magnitude of the integrated signal is within the integrator's full scale range, the capacitor will be fully discharged during this phase, causing a pulse to appear on the EOC/POLARITY line. The table in Figure 8 shows the linear relationship between (1) the integrated input signal, and (2) the elapsed time between the Φ3 and EOC pulses.

If the magnitude of the integrated signal exceeds the integrator's full scale range, EOC will not be issued. In such a case, a pulse must be issued on the RESET line after the maximum reference integration time has elapsed; this will cause the overrange condition to be cleared by the autozero circuit.

Timing Resolution and Code Conversion

The resolution of the analog-to-digital conversion may be established at any desired level continuously up to 16 binary bits or 4 full BCD digits plus sign. Linearity will be 0.001% FSR regardless of the resolution selected. Selection of resolution is accomplished by specifying the external counter's clock rate in accordance with the following relationship:

$$\text{Fclock} = \frac{B^{(n-1)}}{T} \quad \text{(the maximum counts at } \pm\text{full scale)}$$

where n is the desired resolution (including the sign bit), B is the counting base (normally 2 or binary) and T is the maximum reference integration time. As an example, for 15-bit binary resolution with 60 Hz power line:

$$\text{Fclock} = \frac{2^{(15-1)}}{8.33\text{ ms}} = 1.966\text{ MHz}$$

A 2 MHz clock may be used for convenience in this case, which will slightly increase the resolution with no change in linearity. As a second example, for a full 4 digit BCD display plus sign with 50 Hz power line:

$$\text{Fclock} = \frac{10^{(5-1)}}{10.0\text{ ms}} = 1.00\text{ MHz}$$

Other coding, such as two's complement, can be established by simple logic at the counter's output.

Calibration

The MP2316A is inherently stable, and in most applications will not require recalibration more often than every six months. When recalibrating the system, adjust offset before adjusting range.

Offset Adjustment

RTI offset may be adjusted to zero via an external potentiometer installed between AUTOZERO RETURN and the SIGNAL RETURN (see Figure 9); RTO offset may be adjusted via a time delay between 03 and the start of the external software or hardware counter. With a 0V input signal, adjust the offset signal via the selected method(s) so that the reference integration time is within the desired tolerance (e.g., within one or two clock periods of the counter start).

Range Adjustment

Range may be adjusted via a potentiometer installed between the PGA OUTPUT pin and the INTEGRATOR INPUT pin (see section on gain programming). It is recommended that an input voltage of roughly 10% less than full scale be used during this adjustment procedure to avoid overrange conditions during adjustment. Adjust the range so that the dual-slope-derived reference integration time, as shown by an external counter, is proportional to the input voltage to within the desired tolerance.

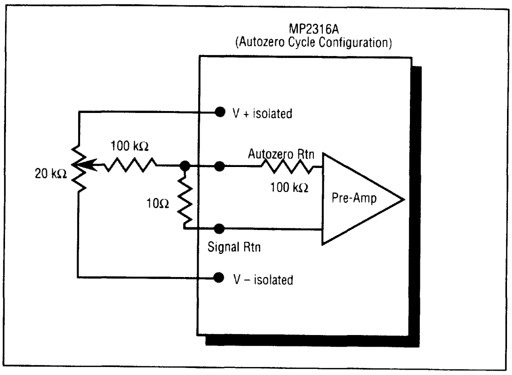


Figure 9. Optional RTI Offset Compensation.

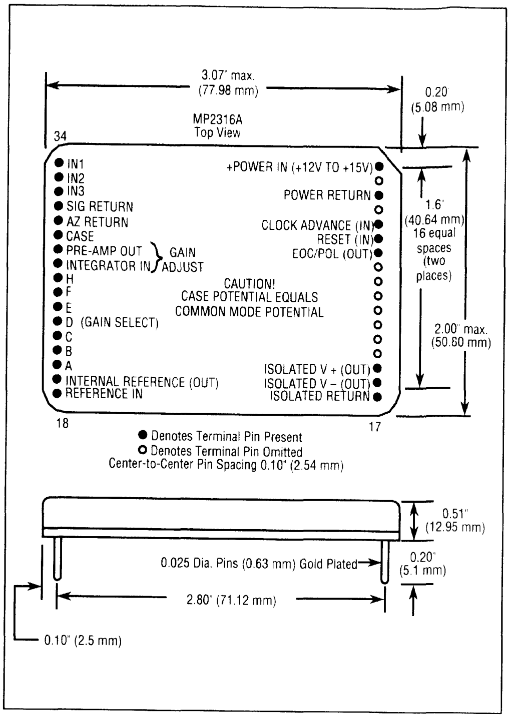


Figure 10. Mechanical and Pinout.

Ordering Guide

Specify **MP2316A**

Notice: The Analogic MP2316A is protected under one or more of the following U.S. patents and others pending:

3,051,939; 3,054,910; 3,316,547; 3,649,924; 3,750,146

Amplifiers, and Sample-and-Hold Amplifiers

Selection Guide

Amplifiers, and Sample-and-Hold Amplifiers

Glossary of Terms

Acquisition

The time it takes the S/H amplifier to start tracking the input signal. It is measured as the maximum elapse time between application of the sample command and the point at which the output starts to track the input within a specified accuracy regardless of the previous state of the output or the magnitude or polarity of the input. See Figure 1.

Aperture Delay Time

The time delay between the HOLD command and the actual start of the HOLD mode. In reference to the SAMPLE mode this is called the turn-off time. See Figure 1.

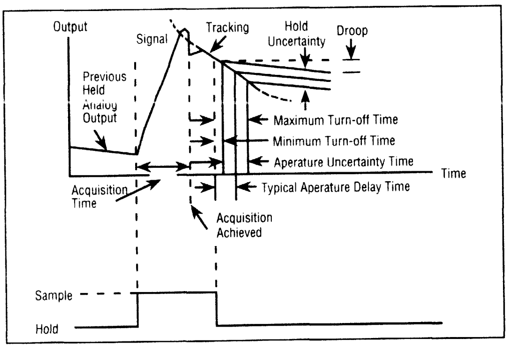


Figure 1. S/H Amplifier Terminology

Aperture Uncertainty

A specification indicating how much the aperture delay time varies. It is measured as the difference between the maximum turn-off time and the minimum turn-off time. See Figure 1.

Common-Mode Range

Common-mode range for a particular A/D converter is the highest value common mode voltage that may appear at the input for which the converter will perform within specifications.

Common-Mode Rejection

Common-mode rejection (CMR) applies to amplifiers, A/Ds, multiplexers, and other analog-input circuits.

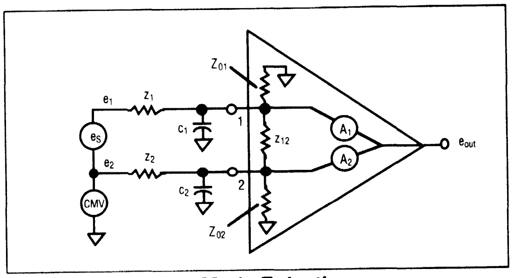


Figure 2. Common-Mode Rejection.

A_1 and A_2 are the gain magnitudes between the output and inputs 1 and 2. Z_{01} and Z_{02} are "common-mode" input impedances at terminals 1 and 2. Z_{12} is "differential" input impedance between terminals 1 and 2. Z_1 and Z_2 are source impedances. C_1 and C_2 are capacitances from the inputs to ground, including input capacitance of the device itself. e_S is differential input signal = (e_1-e_2). Common-mode voltage (CMV) = e_1-e_S.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the CMV to the contribution to the output due to CMV alone–i.e., CMV / Δe_{out} where Δe_{out} is referred to the input. This parameter is usually expressed in dB, via.:

$$\text{CMRR} = 20 \log_{10} \left(\frac{\text{CMV}}{\Delta e_{out}}\right).$$

For the device alone, then:

$$\text{CMRR} = 20 \log_{10} \left(\frac{1}{A_1-A_2}\right).$$

Dielectric Absorption Error

Dielectric absorption error is the decaying of the HOLD voltage on the HOLD capacitor due to the charge redistribution within the capacitor dielectric. This error occurs as a result of rapidly charging the HOLD capacitor and then disconnecting the charging source. The output voltage will decay according to the following relationship:

$$\Delta E = E_S K \log_{10}\left(\frac{t_s + t_h}{t_s}\right)$$

where:

ΔE =	Output voltage error
E_S =	Capacitor voltage change
K =	Empirical constant for Hold capacitor dielectric ($K = 1.5 \times 10^4$ for polystyrene capacitor)
t_s =	Sample time
t_h =	Hold time

Example: For a 20V step, a Sample time of 2 µs, and a Hold time of 5 µs, ΔE = 1.5 mV

Digital Control Specifications

These are specifications for interfacing the digital control signals to the S/H and include: the logic type (e,g,, 1 = SAMPLE, 0 = HOLD); and the required speed of the rise or fall time between SAMPLE and HOLD modes.

Distortion

Unwanted output signals generated as a result of nonlinearities in the sample and hold.

Droop Rate

The maximum rate of change of the output voltage in the HOLD mode.

Feedthrough Rejection

The ratio, in dB, of a specified input signal to the resultant output signal, during HOLD, over a stated frequency range.

Full Power Bandwidth

The highest frequency at which an analog circuit will track a sinusoidal signal large enough to drive the output to its rated full-scale value at its maximum rated power. The equation is as follows:

$$f = \text{Slew Rate} / 2\pi e_{fs}$$

where

f =	Full Power Bandwidth and
e_{fs} =	Rated Full Scale Output

Gain Accuracy

The maximum amount that the actual voltage gain deviates from the nominal value expressed as a percentage of that nominal value. This takes into account the effects of temperature variations, power supply variations, and drift with time, if significant.

Input Impedance

Specified as a nominal resistance in parallel with a capacitance value, given for the SAMPLE mode. If the HOLD mode impedance is significantly different, it will also be given. Input impedance is given at maximum rated input voltage.

Input Signal Range

The acceptable input signal levels, over the full power bandwidth, for which the amplifier or S/H will maintain rated linearity.

Isolation Amplifier

A circuit that typically accepts a low level signal, often in the presence of a high level common mode voltage from a transducer, and amplifies it to produce a clean, accurate output signal.

Linearity

In sample mode, linearity is a measure of how accurately the output tracks the analog input signal. In the hold mode, it refers to the pedestal offset which varies over the input signal range.

Offset Drift

The worst case variation in output offset voltage due to changes in ambient temperature, power supply voltage, and drift with time.

Output Offset Voltage

The maximum value of output voltage observed when sampling zero input at a stated temperature and power supply.

Output Voltage Swing

The rated nominal output voltage range into a specified minimum load impedance.

Overload Recovery Time

The time required for the circuit to return to linear operation, within a stated tolerance, after removal of a sustained input that was large enough to drive the circuit into complete saturation (i.e., a condition in which further increase in the input did not significantly increase the output).

Pedestal Offset Error

An offset error caused by switching to the HOLD mode. It is affected by a number of parameters, including the capacitance of the mode control switch, the HOLD mode command signal level, the analog input signal level and the sample rate. The pedestal offset error may be nonlinear.

Sample and Hold Amplifier

Sometimes called a track and hold amplifier, this is a circuit used to monitor a rapidly changing analog signal and, upon command, hold that signal level for processing by another circuit, typically an ADC. The S/H operates in two sequential modes, SAMPLE and HOLD, as determined by the state of a switch at the input to the amplifier which is controlled by an external digital control signal. In SAMPLE mode the switch is closed, the input signal is connected to the amplifier and the output tracks it very closely. In the HOLD mode the switch is open, the input is disconnected from the amplifier and its level at the time of disconnect is maintained by a capacitor across the input. See Figure 3.

Settling Time

The maximum time required for the output to track the input to within the specified accuracy after a full range step change (while in SAMPLE mode for S/H amplifiers).

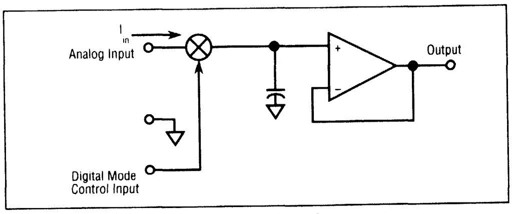


Figure 3. S/H Amplifier Block Diagram.

Slew Rate

The maximum slew rate is the fastest rate of change of the output of the amplifier. The output changes most rapidly when a step change is applied at the input sufficient to drive the output from one end of its range to the other. (S/H amplifiers are characterized in the sample mode.)

Small Signal Bandwidth

The maximum small signal bandwidth is the highest frequency at which an amplifier will track, to within 3 dB of the low frequency response, a sinusoidal signal of less than the slew rate limited amplitude.

Turn Off Time

See aperture delay time.

Voltage Gain

The nominal ratio of output to input.

MP227A

Precision Isolation Amplifier

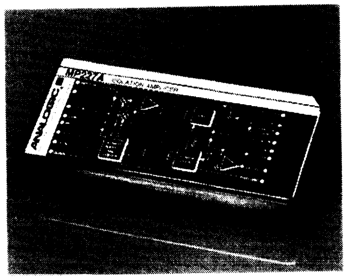
Replaces Relays and Filter Elements in Multichannel DASs

Introduction

The Analogic MP227A is a precision isolation amplifier that provides an unparalleled cost-effective combination of linearity, stability, and isolation. It is designed primarily to replace relays and filter elements in multichannel data acquisition systems. However, its unique features make it attractive wherever low-level, low frequency signals must be applied in the presence of severe common mode interference.

The MP227A offers user-selectable gains from 10 to 1000, input full-scale voltage ranges from ±10 mV to ±1V, 3-pole (60 dB/decade) filtering from 5 Hz, extremely good linearity, superb common-mode rejection, and very low drift. All parameters are commensurate with A/D conversion at levels up to 13 bits.

The MP227A includes an internal power oscillator and isolated supply so that no external drivers are needed. The isolated power (±4V nominal) can be used for open thermocouple indication or offsetting strain gauge inputs.



Features

- High Common Mode Rejection– 170 dB
- Excellent Linearity– 0.0075%
- Selectable Input Range– ±10 mV FS to ± 1V FS
- Low Noise– <0.5 μV RMS
- Low Drift– 3.0 μV RTI per Month
- Built-in 3-pole Filtering
- Built-in Oscillator/Driver

Applications

- Thermocouple Temperature Measurement
- Weighing Systems
- Strain Gauge Measurements
- Remote Data Acquisition and Precision Telemetry Systems
- Microvolt and Millivolt Level Measurements
- Replacement for Classical Instrumentation Amplifier

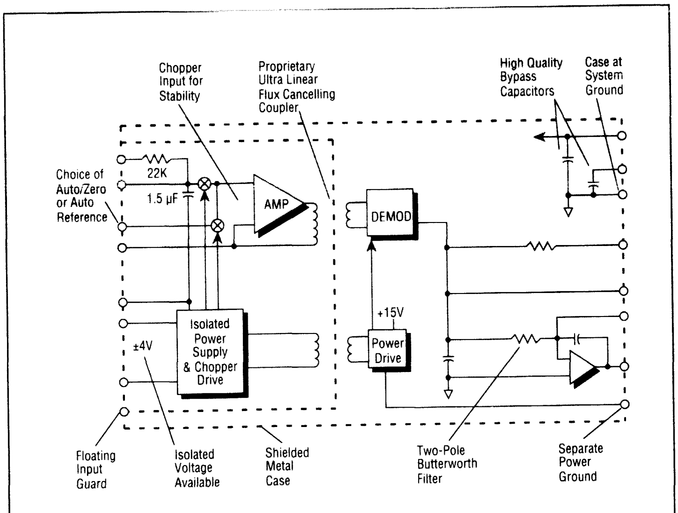


Figure 1. MP227A Block Diagram.

ANALOGIC®
The World Resource for Precision Signal Technology

MP227A

Specifications

All specifications guaranteed at 25°C unless otherwise noted.

ANALOG INPUT

Gain Range
10 to 1000, Non-inverting, Resistor Programmable; Optimized for Gains of 50 to 500

Non-linearity
±0.0075% FSR Max. at G = 50 to 500
±0.01% FSR Max. at G = 1000
±0.05% FSR Max. at G = 10

Input Amplifier Type
Isolated Chopper

Linear Differential Input Voltage Range
±10 mV to ±1V Full Scale

Maximum Safe Differential Input Voltage
16V RMS Continuous, without Damage

Common Mode Isolation Voltage
1000 VDC, 750V RMS Max.

Common Mode Rejection Ratio
At DC, with G =100 & 1000, 166 dB Min.; 1 kΩ Source Unbalance
At 60 Hz, with G = 100 & 1000, 176 dB Typ., 160 dB Min.; 1 kΩ Source Unbalance

Common Mode Impedance
10,000 MΩ / / 80 pF

Differential Input Impedance
At DC, 10 MΩ Min.; at AC, Low-pass Filter of 22 kΩ and 1.5 μF

Overload Input Impedance
22 kΩ, at 50/60 Hz

Input Bias Current
0.5 nA Typ., 3.0 nA Max.; Bias Current Increases if Open Input Indicator Circuit Used

Offset Voltage
At G = 10, ±1 mV Typ., ±5 mV Max.; at G = 1000, ±150 μV Max.; all Referred to Input (RTI); Offset Voltage may be Determined by Interpolation for Other Gain Values

Voltage Noise (0.01 to 5 Hz)
At G = 10, 1.5 μV RMS Max.; at G = 100 and 1000, 0.5 μV RMS Max.; RTI

Bandwidth[1]
DC to 5 Hz Nom.; 6 dB Down at 5 Hz

Overall Filtering[2]
3-pole, 60 dB/Decade Roll-off (–60 dB at 50 Hz)

Input Filter
1-pole RC, 3 dB Cut-off at 5 Hz

Output Filter
2-pole Butterworth, 3 dB Cut-off at 5 Hz

ANALOG OUTPUT

Voltage Range
±10V Full Scale

Output Impedance at DC
0.1Ω

Maximum Load
±5 mA and 500 pF

Output Protection
Continuous Short Circuit to Ground

Output Chopper Noise (1 MHz BW)
±1 mV p-p Spike at Approximately 10 kHz[3]

STABILITY

Gain Tempco
At G = 10 and 100, ±25 ppm FSR/°C Max.; at G = 1000, ±35 ppm FSR/°C Max.; Exclusive of External Gain Setting Resistor

Offset Voltage Tempco
At G = 10, ±5.0 μV/°C Max.
At G = 100, ±1.7 μV/°C Max.;
At G = 1000, ±0.5 μV/°C Max.;
All RTI

Bias Current Tempco
100 pA/°C Max., at 25°C;
Doubles Every 10°C Max.

Power Supply Sensitivity
At G = 1000, ±2.0 μV/%;
at G = 10, ±10 μV/% Max.; RTI

Warm-up Drift (5 Minutes)
Within 2 μV RTI Typ. at G = 1000

Long Term Drift
3.0 μV RTI/Month Typ.

ISOLATED POWER SUPPLY OUTPUT

Voltage
±4 VDC Nom., with respect to INPUT LO

Current
±3 mA Full Load

Regulation
12%, No Load to Full Load

Ripple
60 mV p-p at 10 kHz

INPUT POWER SUPPLY REQUIREMENTS

+15V, ±3%
3 mA, No Load

–15V, ±3%
5 mA, No Load

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +70°C

Storage Temperature Range
–55°C to +85°C

Relative Humidity
0 to 85% Non-condensing up to 40°C

Dimensions
1.2" x 2.8" x 0.5"
(30 mm x 70 mm x 12 mm)

Shielding
RFI: 6 Sides; EMI: 5 Sides

NOTES:

1. Modifications for bandwidths from DC to 100 Hz, or optimized for specific settling times are available on special order. Please contact factory.
2. Filter nodes are externally accessible to allow modification of characteristics.
3. Output Chopper noise can be reduced to negligible level by suggested output multiplexer circuit.

Specifications subject to change without notice.

OPERATION DATA

Application

The MP227A was designed as an economically competitive and functionally superior alternative to the relay multiplexing circuits traditionally used in multichannel data acquisition systems. In a typical thermocouple system, the MP227A replaces three functional blocks for each channel – the input filter and a dual relay, as well as the common channel high gain amplifier – and permits high-level, solid-state multiplexing to be used for low cost and high reliability.

The MP227A provides significantly better isolation and common-mode rejection than low-level relays and it puts the gain at a point in the system where the bandwidth is lowest (prior to multiplexing), thereby reducing total system noise. Even where multiplexing is not used, the unusual combination of performance and price makes the MP227A attractive for a wide variety of industrial applications.

When many MP227As are used in a system, a high-speed, high-level analog multiplexer switches the MP227A outputs to a common analog output bus for subsequent A/D conversion. Any high precision isolation amplifier/filter used in such a configuration has an inherent error source of sizable magnitude that is often overlooked, ignored, or simply unknown; that is, dumped charge effects. This Application Note discusses the problem, the solution, and the fringe benefits.

Dumped Charge

Figure 2 shows the apparently straightforward connection of multiple amplifiers/filters and multiplexer to a common A/D converter.

Each time the multiplexer in Figure 2 switches channels, for instance, from Channel 1 to Channel 2, the

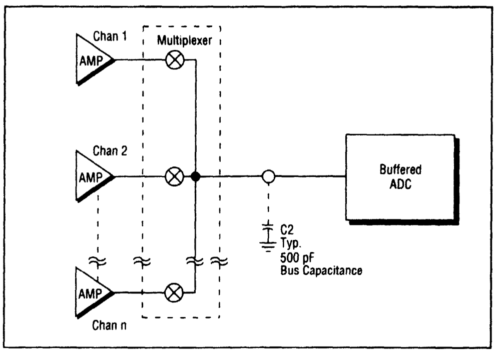


Figure 2. Multiplexing Amplifier Outputs.

Channel 1 output appears across C2, the capacitance of the output bus. The output stage of Channel 2 must absorb that dumped charge before it can reach a true final value dependent only on its input. The exact magnitude of the dumped charge is not important; what is significant is that the Channel 2 amplifier may be forced to deliver a peak instantaneous current beyond its design specifications.

The dumped charge (Q) is defined as, Q = idt,

where i = C dv/dt

In a typical example, the outputs of the two channels could be at the extreme ends of the range.

Channel 1 output = +10V.

Channel 2 output = −10V.

This makes the voltage difference (dv).

dv = 20 volts.

Assume that the capacitance of the output bus C2 is about 500 pF, and a reasonable turn-on time for an analog switch is 100 ns, or,

$C = 500\ (10^{-12})$

$dt = 100\ (10^{-9})$

Solving first for the current and then the dumped charge, gives:

$$i = C\ (dv/dt) = \frac{500(10^{-12})}{100\ (10^{-9})}\ 20 = 100\ \text{mA}$$

Q = idt = (100)(10–3)(100)(10–9) = 10,000 pico Coulomb

Under these conditions, IC op amps, such as the popular 741, have been found to have full-scale current excursion lasting as long as a microsecond.

If the design factors allow a conventional IC output stage to drive the multiplexer instead of a high precision amplifier with an output/filter stage, no real harm is done by the dumped charge. The amplifier eventually recovers and C2 charges to the new value. The recovery time constant is the ON resistance of the multiplexer switch and C2

for R on = 300Ω

C2 = 500 pF

$T = (300)(500)\ 10^{-12} = 0.15\ \mu s$

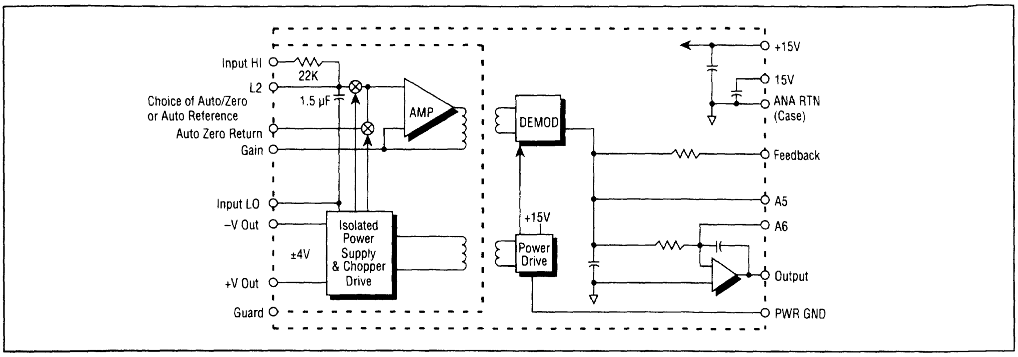


Figure 3. MP227A Isolation Amplifier Functional Block Diagram.

In high resolution systems, ten time constants should be allowed to reach a voltage within 0.005% of final value. Therefore, the actual time should be 1.5 µs.

The 1.5 µs settling time required in this example is usually less than the settling time of the conventional buffer amplifier at the multiplexer output, and the dumped charge effect can be safely ignored. The dumped charge cannot be ignored, however, when high precision amplifiers employing output filters are required.

The Problem

Many isolation and/or instrumentation amplifiers do not include an output filter. On the other hand, the MP227A has an integral two-pole Butterworth filter in the output stage. The feedback element of the MP227A is a capacitor, and a sudden voltage step at the amplifier output, such as the dumped charge, presents a problem.

The dumped charge demands excessive current in too short a time and causes the amplifier to momentarily open-loop. The summing node changes to a large voltage, inducing current flow in the input resistor and causing an extraneous charge on the feedback capacitor.

This error source has produced observed errors as large as 0.05% in typical applications.

The Solution

Figure 4 shows the addition of a single-pole filter (R1,C1) at the output of each MP227A and ahead of the multiplexer. C1 of the succeeding channel now absorbs the charge accumulated on C2 from the preceding channel. The MP227A no longer sees a step but a well controlled exponential change, well within its capabilities. Hence, the output stage in the MP227A does not open-loop, and no spurious charge is placed on the feedback capacitor.

The best results are obtained with a time constant between 0.25 and 0.5 µs. This must be short for two reasons: 1) a settling time of up to 10RC does not significantly add to multiplexer settling time; and 2) the recovery time is sufficiently short for final values that are independent of the duty cycle involved in reading a channel.

R1 should be between 50 and 270Ω; this value is kept intentionally low to reduce voltage divider error (R1 + Ron relative to Rin of the follower at the multiplexer output) to an insignificant level. These values of R1 yield values for C1 between 10,000 pF and 1,000 pF which is an acceptable range for C1. In the capacitive voltage divider, formed by C1 and the bus capacitance C2, as C1 decreases in size relative to C2, the initial voltage transferred to C1 by a succeeding channel approaches its final value and leaves a smaller exponential rise portion.

R1, C1 MUST BE INCLUDED FOR ALL HIGH RESOLUTION (>12 BITS) APPLICATIONS OF THE MP227A.

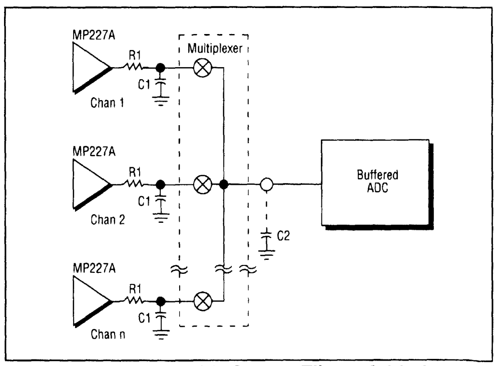


Figure 4. MP227A with Output Filters Added.

Fringe Benefits

Noise spikes inherent in the design of high performance isolation amplifiers are attenuated by 10 dB or more by the R1 C1 output filter.

The superior isolation of the MP227A is provided by transformer coupling. A modulator/demodulator is used in the analog signal path and is driven by an integral chopper/power driver. It is impossible to avoid some stray capacitance between the driver circuitry and the output. Careful design and layout of the MP227A has reduced the resulting output noise spikes caused by stray capacitance to 1 mV p-p, which is 0.01% relative to 10V FS, when measured over a bandwidth of 1 MHz. The noise spikes repeat at 20 kHz, or twice the nominal 10 kHz frequency of the MP227A chopper driver.

If the output filter time constant (R1 C1) is equal to 0.5 μs, then:

$fc = 1/2\pi RC$

$= 333$ kHz

This low cut-off frequency ensures that the output spikes, over an effective bandwidth in excess of 1 MHz, are attenuated 10 dB or more, which is enough to reduce this error source from .01% to a negligible level.

USING THE MP227A

Offset Adjustment

Provision is made for offset adjustment on the MP227A Precision Isolation Amplifier by connecting a 25k or 50 kΩ (100 ppm/°C or better) multi-turn potentiometer (R2) with a 1 MΩ resistor as shown in Figure 5. To adjust, momentarily short INPUT HI, INPUT LO, and AZ RTN to the output ANA RTN and set the offset potentiometer for zero output at the OUTPUT terminal.

Setting the MP227A Gain

The gain of the MP227A may be set to any value from 10 to 1000 by connecting an external resistor (RG) between the GAIN and INPUT LO terminals as shown in Figure 5.

$$\text{Gain} = \frac{10.375 \times 10^3}{RG\Omega}$$

An RN55E or better resistor is recommended for temperature stability. Untrimmed, the absolute gain will be within +2% and −3% of the calculated value.

Gain Trimming

The gain may be deliberately fine-trimmed, if desired, by connecting a 500Ω (100 ppm/°C or better) potentiometer (R1) between the FEEDBACK and OUTPUT terminals as shown in Figure 5. R1 compensates for the tolerance of RG plus the unit-to-unit gain variability (3%) between multiple MP227As. This also allows standardization of the outputs of multiple MP227As to a common full-scale range. For volume production where cost is a factor, the trimpot may be replaced with a fixed resistor selected during final testing.

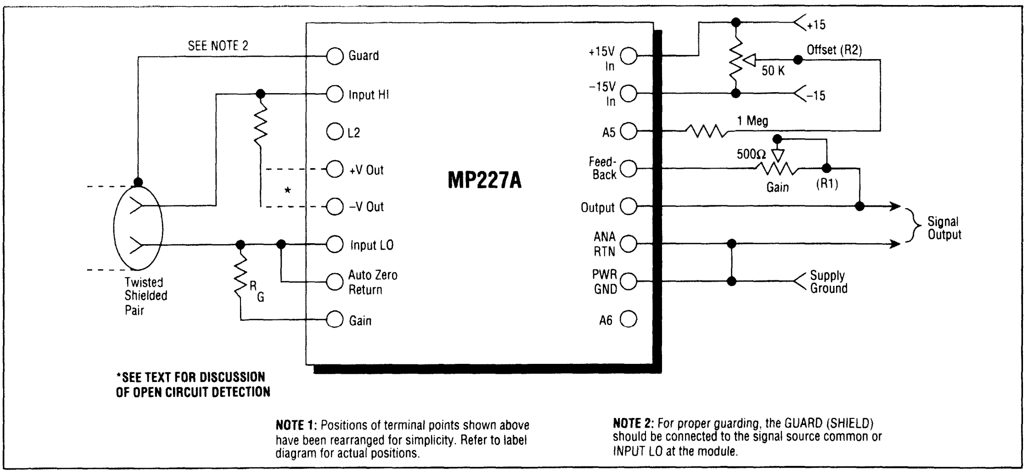


Figure 5. Typical External Connections – MP227A

Auto-Zero Return

The signal that is amplified by the MP227A is actually the difference between the INPUT LO and the Auto-Zero (AZ) voltages. For normal operation, tie the AZ terminal directly to the INPUT LO terminals. In some applications, it may be convenient to offset the input deliberately by an amount that exceeds the range of the OFFSET trimpot (for example, to obtain expanded scale operation or to cancel out the initial or "tare" output of a load cell). To do this, connect the AZ terminal to a source of voltage equal to the desired offset, with noise performance and stability at least as good as the signal source.

Observe that both the INPUT HI signal and the AZ signal (if any) are measured with respect to the INPUT LO terminal. For best linearity, each signal must be within ±1V of INPUT LO.

Open Input Indication

The user-accessible isolated power supply voltages make it possible to use a simple open input indication network. Connect a resistor on the order of 180 MΩ to the INPUT HI and either the +4V or –4V isolated power output terminal. This network produces a bleeder current of approximately 20 nA through the input source circuitry. If the source should open, this bleeder current will drive the MP227A output into a saturated state. The speed of this response is a function of the MP227A gain setting and input time constant.

Multiplexing MP227As

The outputs of multiple MP227As may be multiplexed to a common analog line as indicated in Figure 4. A single RC filter ahead of each MUX is suggested.

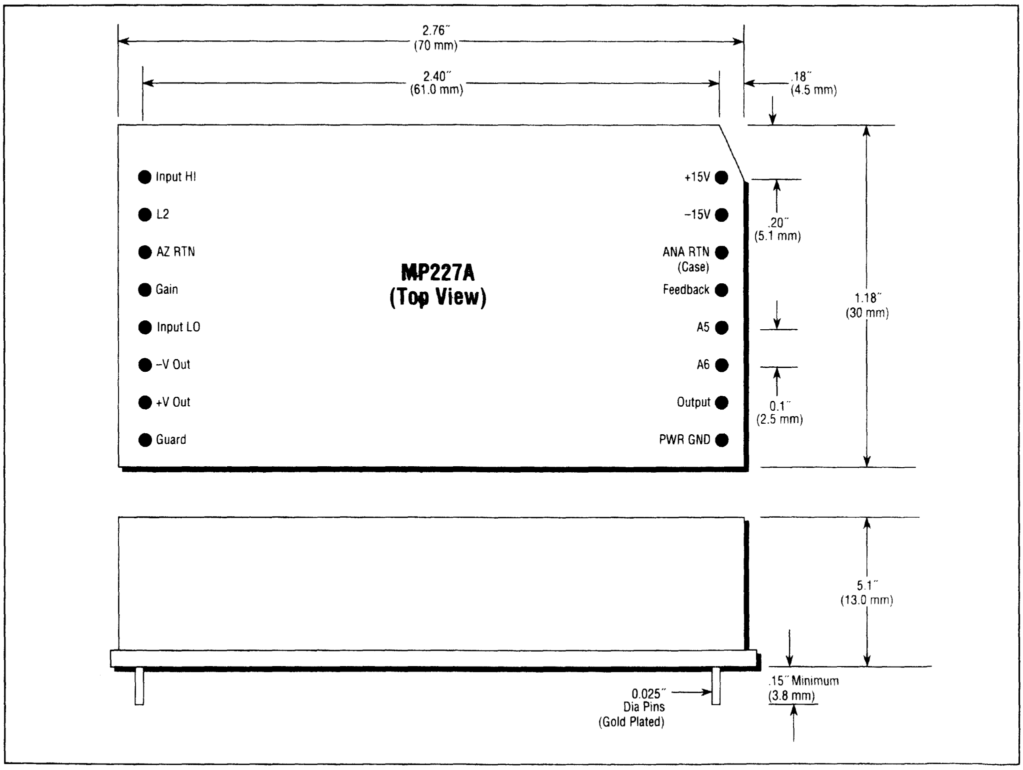


Figure 6. MP227A Mechanical & Pinout.

Ordering Guide
Specify **MP227A**

High-Speed, 225 ns High Accuracy Wideband Sample-and-Hold Amplifier

with ±0.003% Nonlinearity

Introduction

The SHA2200 is a fast precision sample-and-hold amplifier, featuring an acquisition time of 225 ns with ±0.003% nonlinearity. The SHA2200 provides an optimal combination of speed and precision, as evidenced by its low aperture uncertainty of 10 ps RMS, excellent linearity, low feedthrough of –84 dB at 1 MHz, and its 2 MHz full power bandwidth. In fact, this sample-and-hold amplifier was designed for Analogic's ADC3110 A/D converter, which features 14-bit performance with a 2 MHz sampling rate. Accepting a bipolar ±5V input signal, the SHA2200 has a high input impedance (1 MΩ), low input capacitance (15 pF), and low noise (30 µV RMS). The superior performance of the SHA2200 makes it an ideal choice for multiplexed, high-speed, high resolution applications such as DSP systems, automatic test equipment, and industrial data acquisition and control systems.

In a multiplexed data acquisition application, the SHA2200 provides not only high speed and high resolution but also the required high input impedance. Voltage divider error, caused by the multiplexer's ON resistance in series with the input impedance, is negligible with the SHA2200 because of its 1 MΩ input impedance. Thus, the SHA2200 sample-and-hold is an excellent choice for interfacing to CMOS or FET analog multiplexers.

The SHA2200 features a low droop rate of 5 µV/µs, making it particularly well suited for 14-bit A/D converters. In the hold mode, the SHA2200 will hold an input signal to ±0.006% of full scale for 120 µs!

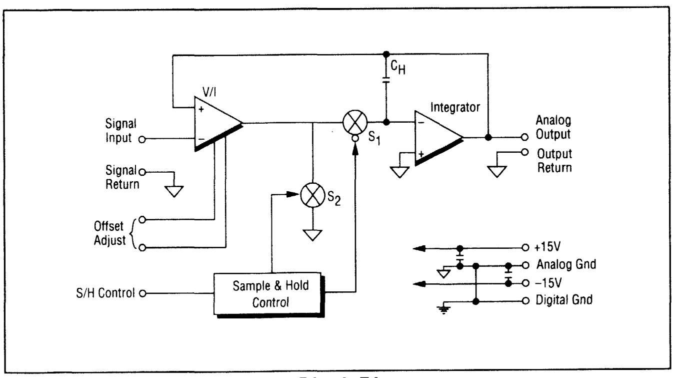


Figure 1. SHA2200 Simplified Block Diagram

Features

- ❑ Fast Acquisition (225 ns)
- ❑ Low Aperture Uncertainty (10 ps RMS)
- ❑ 2 MHz Full Power Bandwidth
- ❑ Low Feedthrough (–84 dB at 1 MHz)
- ❑ Excellent Linearity (±0.003%)
- ❑ High Input Impedance (1 MΩ)
- ❑ Low Input Capacitance (15 pF)
- ❑ Low Droop Rate (5 µV/µs)
- ❑ Ease of Use
- ❑ Low Power
- ❑ 24-Pin Hybrid Package
- ❑ Standard Pinout

Applications

- ❑ Wideband Data Acquisition Systems
- ❑ Simultaneous Sampling Systems
- ❑ Telecommunications
- ❑ Automatic Test Equipment
- ❑ Peak Amplitude Measurements
- ❑ Nuclear Research

SHA2200

Specifications (1)

ANALOG INPUTS

Input Range
±5V Min. (2)

Input Bias Current
100 μA Max.

Input Capacitance
15 pF

Input Impedance
1MΩ

CONTROL INPUT

Logic "0" (Sample)
–0.5V Min., 0.8V Max.

Logic "1" (Hold)
2.0V Min., +5.5V Max.

Required Rise Time
5 ns Max. for Min. Aperture Time

DYNAMIC CHARACTERISTICS

Acquisition Time
225 ns Typ., 250 ns Max. to 0.006% of 10V Input Step

Sample-to-Hold Transient Settling Time
100 ns Max. to 2 mV

Output Slew Rate
100V/μs

Pedestal
±3 mV Max.

Aperture Delay
11 ns Typ., 19 ns Max.

Aperture Uncertainty
10 ps (RMS) Max.

Full Power Bandwidth
2 MHz

Small Signal Bandwidth
20 MHz

Droop Rate
1 μV/μs Typ., 5 μV/μs Max.

Feedthrough —
10 Vp-p at 500 kHz
–98 dB

10 Vp-p at 1 MHz
–84 dB

TRANSFER CHARACTERISTICS

Gain
+1 ±0.005% Typ., ±0.02% Max.

Nonlinearity
±0.0015% Typ., ±0.003% Max.

Offset Error
±5 mV (Adjustable to zero)

Noise (Hold Mode) DC to 1 MHz
90 μV (RMS) Typ., 120 μV (RMS) Max.

Noise (Sample Mode) DC to 1 MHz
30 μV (RMS) Max.

Output Voltage
±5V Min.

Maximum Load
1 kΩ Min. || 50 pF Max. (Including cables)

Dielectric Absorption
±0.005% of Voltage Change (3)

STABILITY (0° TO 70°C)

Pedestal Drift
±10 μV/°C

Offset Drift
±75 μV/°C Max.

Droop Rate
Doubles every 10°C

Warm-Up Time
5 minutes

POWER REQUIREMENTS (4)

±15V Supplies
14.5V Min., 15.5V Max.

+15V Current Drain
33 mA Typ., 40 mA Max.

–15V Current Drain
33 mA Typ., 40 mA Max.

Power Consumption
990 mW Typ., 1.1W Max.

Power Supply Rejection Ratio
±20 ppm FSR/% Max.

ENVIRONMENTAL & MECHANICAL

Temperature Range Rated Performance
0° to 70°C

Storage
–25°C to 85°C

Relative Humidity
0 to 85% non-condensing up to 70°C

Dimensions
1.3" x 0.8" x 0.2" (24-pin double DIP)
(33.02 mm x 20.32 mm x 5.08 mm)

NOTES:

1. All specifications guaranteed at 25°C and ±15V supplies unless otherwise noted.
2. Absolute maximum input range without damage is ±15V.
3. The effect of Dielectric Absorption is a function of the sample and hold time. The SHA2200 is tested with a 250 ns sample time and a 250 ns hold time.
4. It is possible to use power supplies from ±12V to ±18V. Consult factory.
5. For a discussion of how to determine the overall throughput rate for the S/H and A/D converter, refer to page 156 of the Analogic Data Conversion Systems Digest.
6. The derivation of this formula is shown on page 154 of the Analogic Data Conversion Systems Digest.

Specifications subject to change without notice.

System Considerations

Sample-and-hold amplifiers are often used to sample many channels at the same instant in time, such as in seismic data acquisition, and to reduce the time uncertainty (and resultant amplitude error) when digitizing fast time-varying signals. Practical systems have inherent finite sampling apertures; however, the SHA2200 minimizes this time to an aperture uncertainty of 10 ps. Figure 2 illustrates the typical timing of the SHA2200 [5]. If a system uses an A/D converter without a sample-and-hold, the time uncertainty is the conversion time of the A/D converter, which is several orders of magnitude longer than the S/H's aperture uncertainty.

A sample-and-hold is required for a particular A/D conversion application if the input signal is changing fast enough so that the input to the A/D converter changes by more than one LSB during the conversion time. For a sinusoidal signal, the calculation [6] is straightforward:

$$F_{Max} = \frac{\text{LSB}}{(\text{Full Scale Range})\,(2\pi)\,(\text{A/D Conversion Time})}$$

F_{Max} represents the maximum allowable input frequency.

For example, with a 14-bit A/D converter that has a conversion time of 0.5 µs and a 10V full scale range, the maximum signal input frequency without a sample-and-hold would be:

$$\text{FMax} = \frac{10\text{V}/(2^{14})}{(10\text{V})\,(2\pi)\,(0.5\ \mu\text{s})} = 38.8\ \text{Hz}$$

Based on this analysis it is clear that most 14-bit applications would require a sample-and-hold.

By using the SHA2200 sample-and-hold the maximum signal frequency increases dramatically. In applications that use a sample-and-hold, the S/H aperture uncertainty replaces the A/D conversion time in the previous equation:

$$\text{FMax} = \frac{10\text{V}/(2^{14})}{(10\text{V})\,(2\pi)\,(10\ \text{ps})} = 970\ \text{kHz}$$

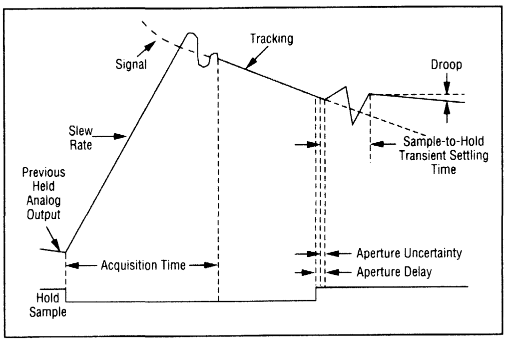


Figure 2. SHA2200 Timing Diagram.

Bypass Capacitor

Two 6.8 µF tantalum bypass capacitors should be installed close to the SHA2200, between +15V and analog ground and between −15V and analog ground.

Adjustments

The SHA2200 allows the input offset error to be externally nulled to zero by connecting a 5 kΩ potentiometer across Pins 17 and 18 as shown in Figure 5. To adjust the offset voltage, place the SHA2200 in the sample mode, short Pins 13 and 15, and set the offset potentiometer such that the output of the S/H is 0V.

The SHA2200 does not include a pedestal adjustment. The pedestal is factory adjusted to <3 mV.

The gain of the SHA2200 is typically within ±0.005% of the nominal ±5V output. This small gain error of the sample-and-hold can be compensated via the gain adjustment potentiometer on the A/D converter following the SHA2200.

Principles of Operation

As shown in Figure 1, the SHA2200 Sample-and-Hold Amplifier uses a summing node technique, which is characterized by the inclusion of the switches within a high gain closed feedback loop. The critical feature of this technique is that is compensates for many of the nonlinearities of the switches and amplifiers.

Several critical components in the design account for the high speed and superb linearity of the SHA2200. The purpose of the voltage-to-current converter is to convert the difference between the input and output voltage to a current at the input of the integrating op amp in the output stage. The storage capacitor exhibits low dielectric absorption, thus allowing it to charge and discharge quickly for high throughput rates. Another advantage of low dielectric absorption is the excellent linearity of the SHA2200. The output amplifier of this sample-and-hold serves as an integrator with low offset error and fast settling time.

The switching sequence is as follows. In the sample mode, Switch S1 is closed, and Switch S2 is opened,

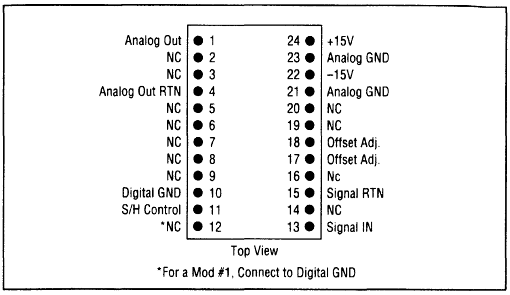


Figure 3. SHA2200 Pinout.

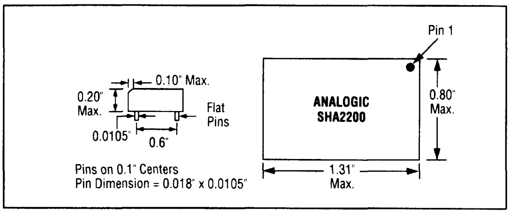


Figure 4. SHA2200 Mechanical Outline

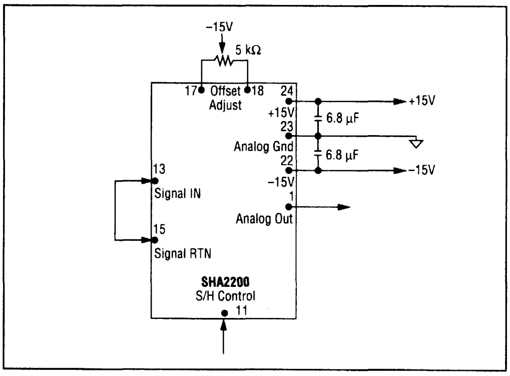


Figure 5. Offset Adjustment.

as the input signal is stored by the integrator. In the hold mode, Switch S2 is closed, and S1 is opened. During the hold mode, Switch S1 exhibits low leakage and S2 has low feedthrough, thus reducing the switching effects on the output signal. These design features make the SHA2200 one of the fastest precision sample-and-hold amplifiers available.

Typical Application

A typical application of the SHA2200 is shown in Figure 6, in which eight input channels are sampled by SHA2200s and multiplexed to an A/D converter. This circuit provides simultaneous sampling, a design requirement in conversion systems in which the phase relationship between different signals is an important parameter. For example, in seismic applications, it is crucial to sample several signals at the same instant in time. The low aperture uncertainty of the SHA2200 allows that instant of time to be known very accurately.

After the hold command is issued, the multiplexer presents the signal levels to the A/D converter as directed by the microprocessor and the control logic. With its speed, linearity, and low feedthrough, the SHA2200 is an excellent sample-and-hold for high speed, high resolution, multiplexed data acquisition systems.

Note that all grounds are connected internally in the SHA2200.

Ordering Guide

Specify
SHA2200

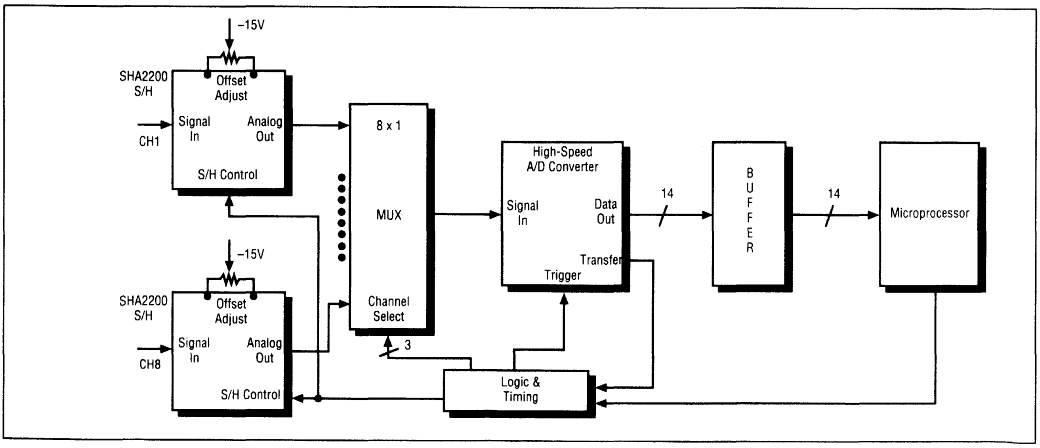


Figure 6. Typical Application for SHA2200.

Very High Accuracy, Low Noise, Sample-and-Hold Amplifier

Designed for High Resolution Data Acquisition Applications

Introduction

The SHA2410 is a high performance hybrid sample-and-hold amplifier designed for high resolution data acquisition applications. The fast acquisition time of 2.5 µs to ±0.0015%, very low aperture jitter of 200 ps, and low feedthrough of 100 dB make it suitable for use with fast 16-bit A/D converters that digitize signals up to 50 kHz. Accepting a bipolar ±5 volt input, the SHA2410 has very low noise, 20 µV RMS, making it an ideal choice for applications requiring 100 dB dynamic range, such as professional audio and nuclear research. In most other open-loop sample-and-hold amplifiers, the linearity is limited by the hold switch performance. The SHA2410 incorporates a unique pedestal compensation circuit to reduce the effects of the hold switch to ±0.003% maximum.

The SHA2410 also features a low droop rate of 0.3 µV/µs, making it particularly well suited for slower high resolution systems. In the hold mode, the SHA2410 will hold an input signal to ±0.0015% of full scale for 500 µs.

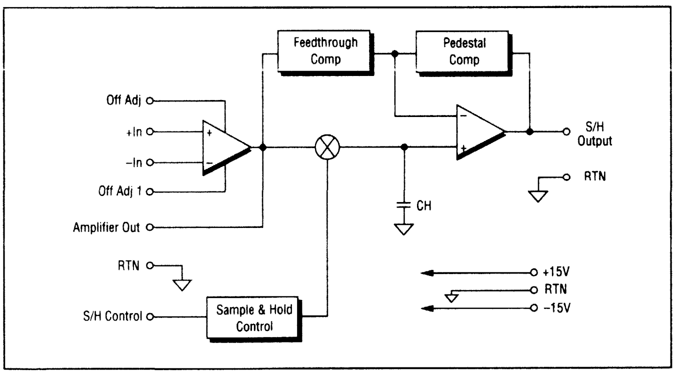
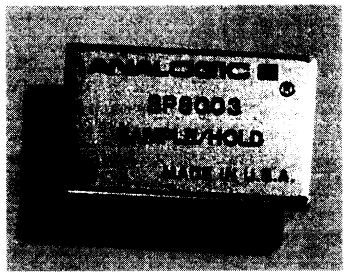


Figure 1. SHA2410 Simplified Block Diagram.



Features

- ❑ Fast Acquisition (2.5 µs)
- ❑ Low Aperture Uncertainty (200 ps RMS)
- ❑ Low Noise (20 µV RMS)
- ❑ Low Feedthrough (–100 dB at 25 kHz)
- ❑ Excellent Linearity (±0.0015%)
- ❑ Low Input Capacitance (5 pF)
- ❑ Low Droop Rate (0.3 µV/µs)
- ❑ Ease-of-Use
- ❑ 14-Pin Hybrid Package

Applications

- ❑ Wideband Data Acquisition Systems
- ❑ Professional Audio
- ❑ Telecommunications
- ❑ Automatic Test Equipment
- ❑ Industrial Process Control
- ❑ Nuclear Research

SHA2410/SP8003

Specifications[1]

ANALOG INPUT

Input Range
±10V [4], ±5V Min. [2]

Input Bias Current
1500 nA Max.

Input Capacitance
5 pF

Input Impedance
10 kΩ

CONTROL INPUT

Logic "0" (Sample)
–0.5V Min., 0.8V Max.

Logic "1" (Hold)
2.5V Min., +5.5V Max.

Required Rise Time
10 ns Max. for Min. Aperture Time

DYNAMIC CHARACTERISTICS

Acquisition Time, Non-Inverting
2.5 µs Max. to ±0.0015% of 10V Input Step

Inverting
2.5 µs Max. to ±0.0015% of 10V Input Step

Sample-to-Hold Transient Settling Time
500 ns Max. to ±0.0015%

Output Slew Rate
10V/µs

Pedestal
±10 mV Max.

Aperture Delay
25 ns

Aperture Uncertainty
200 ps (RMS)

Full Power Bandwidth
150 kHz

Small Signal Bandwidth
2 MHz

Droop Rate
0.02 µV/µs Typ., 0.3 µV/µs Max.

Feedthrough —10 Vp-p at 500 kHz
–100 dB

TRANSFER CHARACTERISTICS

Gain
+1 ±0.005% Typ., ±0.01% Max.

Nonlinearity
±0.0015% Typ., ±0.003% Max.

Offset Error
±5 mV (Adjustable to zero)

Noise (Sample Mode) DC to 1 MHz
20 µV (RMS) Max.

Noise (Hold Mode) DC to 1 MHz
35 µV (RMS) Max.

Output Voltage
±5V Min., ±10V Min.[4]

Maximum Load
2 kΩ Min. || 100 pF Max.

Dielectric Absorption
±0.005% of Voltage Change

STABILITY (0°C TO 70°C)

Offset Drift
50 µV/°C Max.

Droop Rate
Doubles every 10°C

Warm-Up Time
1 minute

POWER REQUIREMENTS [3]

±15V Supplies
14.5V Min., 15.5V Max.

+15V Current Drain
15 mA Typ., 18 mA Max.

–15V Current Drain
15 mA Typ., 18 mA Max.

Power Consumption
450 mW Typ., 540 mW Max.

Power Supply Rejection Ratio
100 µV/% Max.

ENVIRONMENTAL & MECHANICAL

Temperature Range Rated Performance
0° to 70°C

Storage
–25°C to 85°C

Relative Humidity
0 to 85% non-condensing up to 70°C

Dimensions
0.8" x 0.5" x 0.2" (14-pin DIP)
(20.32 mm x 12.7 mm x 5.08 mm)

NOTES:

1. All specifications guaranteed at 25°C and ±15V supplies unless otherwise noted.
2. Absolute maximum input range without damage is ±15V.
3. It is possible to use power supplies from ±12V to ±18V. Consult factory.
4. For ±10V requirements, specify model number SP8003.
5. For a discussion of how to determine the overall throughput rate for the S/H and A/D converter, refer to page 156 of the Analogic Data Conversion Systems Digest.
6. The derivation of this formula is shown on page 154 of the *Analogic Data Conversion Systems Digest.*

Specifications subject to change without notice.

System Considerations

Sample-and-hold amplifiers are often used to sample many channels at the same instant in time, such as in seismic data acquisition, and to reduce the time uncertainty (and resultant amplitude error) when digitizing fast time-varying signals. Practical systems have inherent finite sampling apertures; however, the SHA2410 minimizes this time to an aperture uncertainty of 200 ps. Figure 2 illustrates the typical timing of the SHA2410 [5]. If a system uses an A/D converter without a sample-and-hold, the time uncertainty is the conversion time of the A/D converter, which is several orders of magnitude longer than the S/H's aperture uncertainty.

A sample-and-hold is required for a particular A/D conversion application if the input signal is changing fast enough so that the input to the A/D converter changes by more than one LSB during the conversion time. For a sinusoidal signal, the calculation [6] is straightforward:

$$\text{FMax} = \frac{\text{LSB}}{(\text{Full Scale Range})\ (2\pi)\ (\text{A/D Conversion Time})}$$

FMax represents the maximum allowable input frequency.

For example, with a 16-bit A/D converter that has a conversion time of 17 µs and a 20V full scale range, the maximum signal input frequency without a sample-and-hold would be:

$$\text{FMax} = \frac{20\text{V}/(2^{16})}{(20\text{V})\ (2\pi)\ (17\ \mu\text{s})} = 0.143\ \text{Hz}$$

Based on this analysis it is clear that all 16-bit applications would require a sample-and-hold.

By using the SHA2410 sample-and-hold the maximum signal frequency increases dramatically. In applications that use a sample-and-hold, the S/H aperture uncertainty replaces the A/D conversion time in the previous equation:

$$\text{FMax} = \frac{20\text{V}/(2^{16})}{(20\text{V})\ (2\pi)\ (200\ \text{ps})} = 12.1\ \text{MHz}$$

Bypass Capacitor

Two 6.8 µF tantalum bypass capacitors should be installed close to the SHA2410, between +15V and analog ground and between −15V and analog ground.

Adjustments

The SHA2410 allows the input offset error to be externally nulled to zero by connecting a 100 kΩ potentiometer across Pins 14 and 13 as shown in Figure 5. To adjust the offset voltage, place the SHA2410 in the sample mode, short Pins 1 and 6, and set the offset potentiometer such that the output of the S/H is 0V.

The gain of the SHA2410 is typically within ±0.0015% of the nominal ±5V output. This small gain error of the sample-and-hold can be compensated via the gain adjustment potentiometer on the A/D converter following the SHA2410.

Principles of Operation

As shown in Figure 1, the SHA2410 sample-and-hold amplifier uses an open-loop configuration. The advantage to the open-loop topology is that it achieves a faster acquisition time at a lower cost than other configurations. In Figure 1, it can also be seen that the SHA2410 includes a pedestal compensation circuit, which compensates for the nonlinearity of the switches and amplifiers. Additionally, a feed-through compensation circuit has been added so that true 16-bit performance can be achieved in dynamic systems.

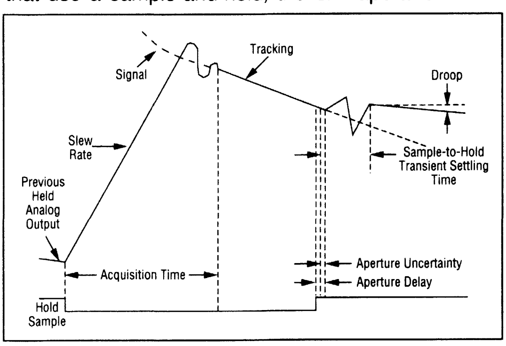


Figure 2. SHA2410 Timing Diagram.

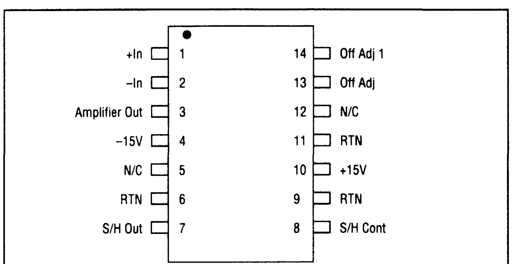


Figure 3. SHA2410 Pinout.

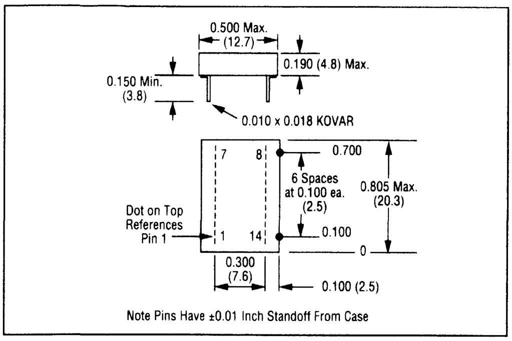


Figure 4. SHA2410 Mechanical Outline.

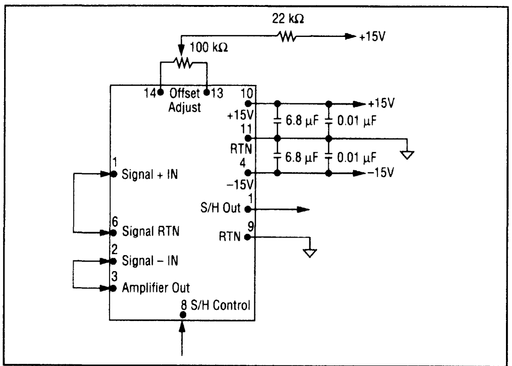


Figure 5. Offset Adjustment.

Applications

The SHA2410 can be used with any user-defined feedback network to provide any desired gain in the sample mode. As shown in Figure 1, the input amplifier is uncommitted to provide the utmost applications versatility. The most common application of the SHA2410 will utilize the connection diagrammed in Figure 6A. In this mode of operation, the SHA2410 will operate as a unity-gain non-inverting amplifier.

The input amplifier has a very high open-loop gain to ensure that gain nonlinearity will be minimized in applications where a gain other than one is utilized. The SHA2410 in a non-inverting gain configuration, as diagrammed in Figure 6B, has a transfer function of 1 + R2/R1 in the sample mode. In the inverting configuration, diagrammed in Figure 6C, the transfer function of the SHA2410 is equal to –R2/R1 when sampling. In the inverting and non-inverting configurations where external resistors are used to set the desired gain, care must be taken to select the appropriate resistor type. Both the initial gain accuracy and gain drift over temperature are functions of the type and matching characteristics of the resistors.

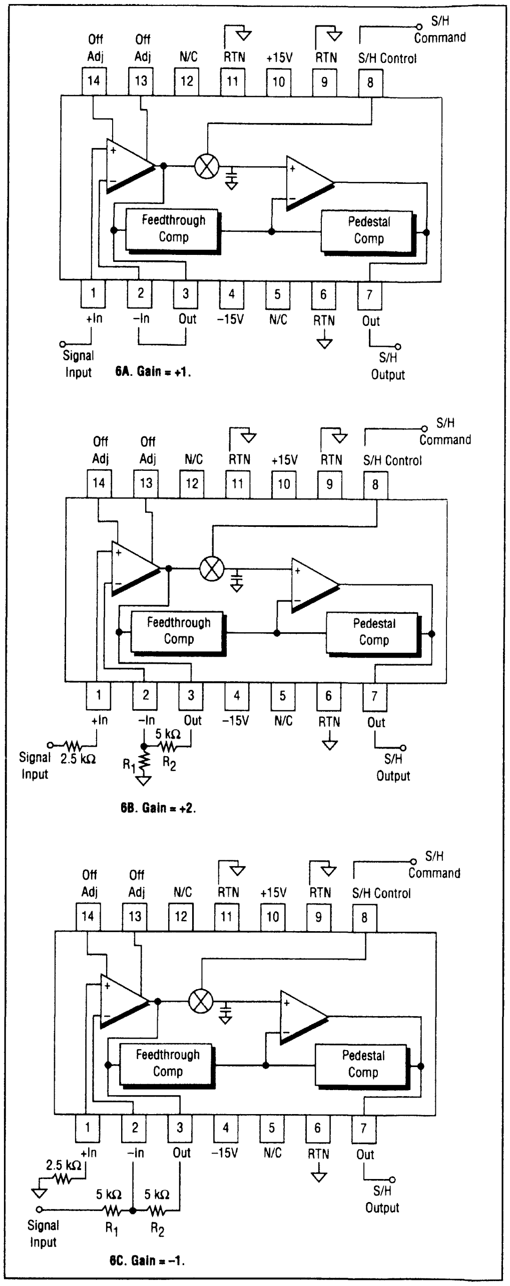


Figure 6. SHA2410 Connection Diagram.

Ordering Guide

High Speed S/H Amplifier 14-Pin DIP

SHA2410	±5V Input
SP8003	±10V Input

DC-to-DC Converters

Selection Guide

Model	Input DC Voltage	Output DC Voltage	Noise Regulation	Plus Ripple	Page
SP7005	+5V	±15V, +5V, –6V	±0.2%	5 mV p-p	127
SP7008	+5V	±15V, +5V, –5V	±0.2%	5 mV p-p	127
SP7015	+5	±15V, +5V	±0.4%	5 mV p-p	127

DC-to-DC Converters

Glossary of Terms

DC-to-DC Converter

A circuit that converts +5V power to highly stable, highly regulated power for bipolar analog circuitry. In addition to stability and regulation, DC-to-DC converter requirements include higher isolation, higher efficiency, EMI and RFI shielding, and short circuit protection. See Figure 1.

Efficiency

A ratio, expressed in percentage, of output power at full load divided by input power.

Isolation

Breakdown voltage between the input and the output.

Reflected Input Ripple Current

Noise fed back to the input of the converter as a result of inductive switching.

Line Regulation

A measure of the ability of the converter to maintain its output voltage when the input voltage changes, e.g., ±0.2% for ±5% input change.

Load Regulation

A measure of the ability of the converter to maintain its output voltage when the load changes, e.g., ±0.2% for no load to full load.

Load transient Recovery

The time it takes the output to settle to its rated value after a specified step change in the load, e.g., 100 µs to settle to rated output with change from 1/2 load to full load.

Peak Transient

The maximum p-p noise level, in a given bandwidth, at the output of a converter.

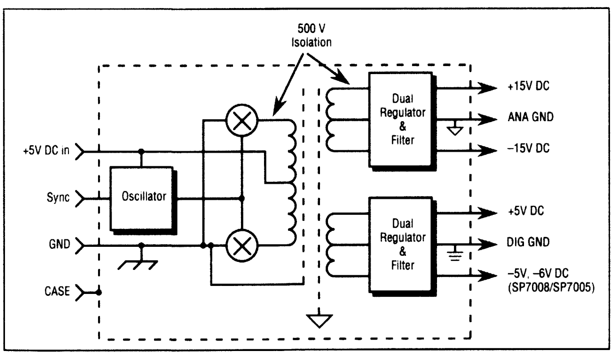


Figure 1. Functional Block Diagram of a DC-to-DC Converter.

SP70XX Series DC/DC Converters

Powers High Performance A/D Converters from a Single +5V Supply

The Analogic SP70XX Series of tightly regulated, isolated, multiple-output DC/DC converters powers high performance 14- and 16-bit A/D converters from a single +5V supply while providing a very low noise-plus-ripple performance of 5 mV p-p. To maintain this high level of performance in a sometimes harsh environment, the SP70XX Series provides capacitive bypassing at both the +5V input and at all supply outputs. To further support the needs of today's high speed, high resolution data conversion products, the SP70XX Series features the capability of synchronizing the chopper frequency to the ADC clock. ***This is the only series of high-performance DC/DC converters with this capability.***

Although the best interfacing approach is heavily dependent on the application, we will try to cover basic design solutions for the majority of high performance data conversion applications. Discussions will include the ADC power requirements, +5V requirement, isolation needs, bypassing, chopper synchronization and temperature limitations.

A/D Converter Supply Requirements

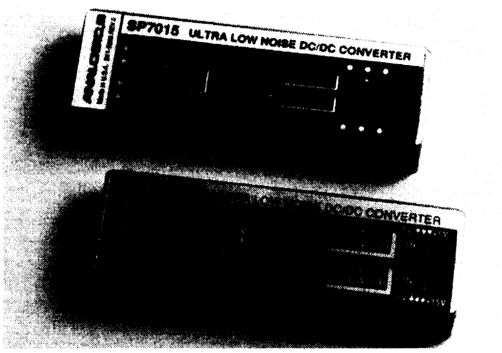
The power supply rejection ratio (PSRR) specification of the A/D converter will determine how tightly regulated the supplies must be. PSRR is the measure of the ADC sensitivity to low frequency[1] variations in the supply voltages and is usually expressed as a change expressed in PPM/percent change in any supply voltage. Frequently overlooked, a poor PSRR will corrupt a system just as quickly as a poor layout. Let us take a look at the implications of the PSRR specification and the ADC supply requirements.

Let us assume that the maximum effect of power supply variations to the output data should be limited to ±1/2 LSB. The equation below will solve for the allowable power supply deviations to the ADC in terms of percent.

$$\text{Max. } \Delta \text{ ADC supply voltage } (\%) = \frac{1 \times 10^6}{2 \times 2^n \times \text{PSRR}}$$

where PSRR is in PPM/%

[1]PSRR is usually specified from DC to power line frequencies (50 or 60 Hz.)



Example: A 16-bit sampling ADC with a PSRR of 400 PPM/percent

$$\text{Max. } \Delta \text{ ADC supply voltage } (\%) = \frac{1 \times 10^6}{2 \times 2^{16} \times 400} = \pm 0.019\%$$

For a 15V supply, the Max. ΔV is 15V x 0.00019 = 2.86 mV (5.7 mV p-p)

This formula places an upper limit to the ADC supply variations, including noise-plus-ripple. Clearly, the lower the PSRR specification, the more immunity to power supply fluctuations the ADC has. A typical Analogic ADC has PSRR spec of 10 PPM/percent. Inserted into the above formula, we find that the typical Analogic ADC can withstand low frequency ripples up to 220 mV p-p.

+5V Input Requirements

In the previous example, it was determined our ADC analog supply requirement was for a maximum deviation of 5.7 mV p-p. This is not to be confused with the absolute voltage, which could have a ±3% tolerance. We're talking about fluctuations in supply voltages. Where are we to find such tightly regulated supplies?

Let us assume that linear supplies have already been ruled out due to size or cost. This leaves DC/DC converters with a noise-plus-ripple specification of less than 5 mV p-p. The next set of specifications to examine is the line and load regulation.

Let us assume a constant load on our DC/DC converter. As the DC/DC converter is usually matched up with an ADC, this is not an unreasonable assumption (high performance ADCs usually exhibit a constant load). If we factor in the Line Regulation specification, we can determine the +5V input requirement to the DC/DC converter.

Simply divide the maximum Δ% for the ADC, found in the PSRR paragraph above, by the line regulation of the DC/DC converter and we have the maximum allowable +5V deviation. In the example above, ±0.019%/0.002 (line regulation of the SP70XX Series) = +5V ±9.5%. The end-to-end formula from the +5V DC/DC converter input to the maximum ADC supply deviation is shown below.

$$\text{Max. } \Delta +5\text{V } (\%) = \frac{1 \times 10^6 \times 100}{2 \times 2^n \times \text{PSRR} \times \text{LR}}$$

where PSRR is in PPM/% and
LR (line regulation) is in %

Clearly we cannot exceed the input limits to the SP70XX of +5V ±5%. This simply means that low frequency deviations into the SP70XX Series are not a factor.

Isolation

In certain instances, such as in the presence of high common mode voltages, it may be necessary to completely isolate the field wiring from the system. Figure 1 depicts such a configuration. The opto-isolation to the ADC trigger helps to maintain the 500V input to output isolation provided by the SP70XX Series. In most applications the isolation will not be required. If this is the case, the +5V supply ground should be brought out separately to the common ground found at the ADC (see dotted line), and the opto-isolation will not be required.

Bypassing

The bypass capacitors inside the SP70XX Series are aluminum electrolytics. Characteristically, this type of capacitor has a high effective series resistance (ESR) and therefore may require some additional bypassing at the supply inputs to the ADC (see Figure 2). This will help ensure the low noise, low ripple performance. A tantalum capacitor, approximately 6.8 µF, in parallel with a 0.1 µF ceramic capacitor, should be placed as physically close as possible to the A/D converter's supply inputs.

In the unlikely event that the +5V input is being driven by a relatively high impedance device, a series coil of approximately 25 µH might be required at the input. Otherwise, the use of series chokes or coils should not be required at either the input or the output of the SP70XX Series.

Sync Input

The heart of the SP70XX Series converters is a CD4047 multivibrator connected in the astable mode with a true 50% duty cycle. If no external syncs have

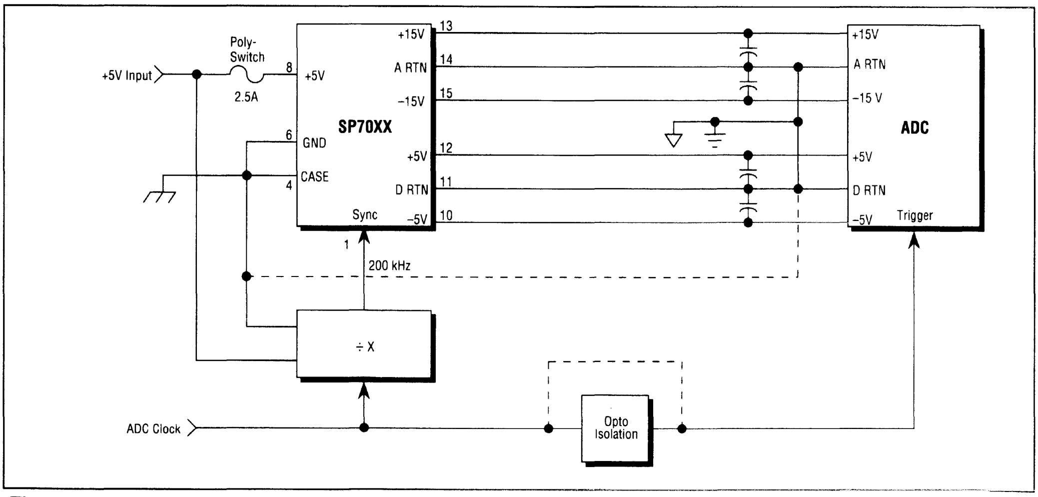


Figure 1. Power Configuration for the SP70XX Series DC/DC Converters. The dotted lines represent the configuration for nonisolated requirements.

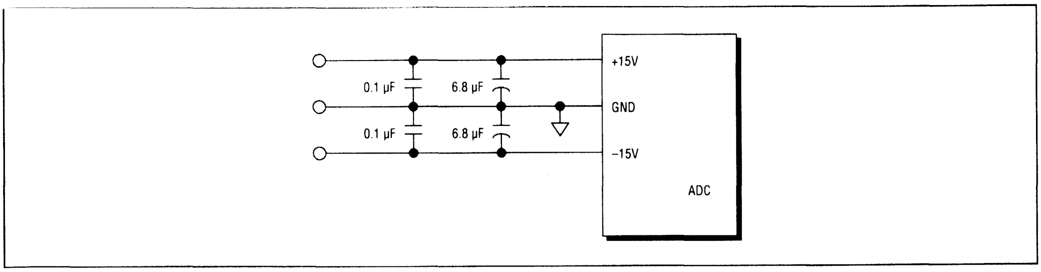


Figure 2. Capacitive bypassing is done at the ADC power inputs.

occurred, the internal time constant is set for the chopper to run at a frequency of 100 kHz ±15 kHz. In many applications this frequency falls directly into the middle of the pass band. Although the ripple out of the DC/DC converter is less than 5 mV p-p, the 100 kHz could show up in the output data in wide dynamic range systems such as 16- to 18-bit ADCs.

The SP70XX Series provides a synchronizing input pin that will override the internal time constant and allow the switching of the chopper to coincide with the HOLD time of the sample-and-hold amplifier. This will allow for any perturbation to settle out before the next sample is taken (see Figure 3). The Sync Input is specified at 200 kHz ±40 kHz and is divided by two internally by the CD4047 to ensure a 50% duty cycle.

SP70XX Series DC/DC Converter Ambient Temperature/Power Derating

Due to the compact size of the SP70XX Series converters, it becomes necessary to pay close attention to the power derating curve shown in Figure 4. As the output load increases from minimum to maximum (no load to full load), the internal temperature predictably rises. The internal temperature rise causes an ambient-to-case temperature differential of +6°C with no load, and +46°C with a full load. The maximum allowable temperature inside the SP70XX Series converters is +85°C; therefore, the maximum ambient temperatures are +79°C and +39°C no load and full load. As the graph above depicts, the derating is linear.

NOTE:

Please note that for OEM applications, a larger package and, therefore, wider temperature ranges are possible. Please consult the factory.

@ P_{out} = 0%: $\Delta T_{ambient\ to\ case}$ = +6°C
T_{Amax} = (85°C –6°C) = 79°C

@ P_{out} = 100%: $\Delta T_{ambient\ to\ case}$ = +46°C
T_{Amax} = (85°C - 46°C) = 39°C

Maximum P_{out} (%) = $-2.5T_A + 197.5$

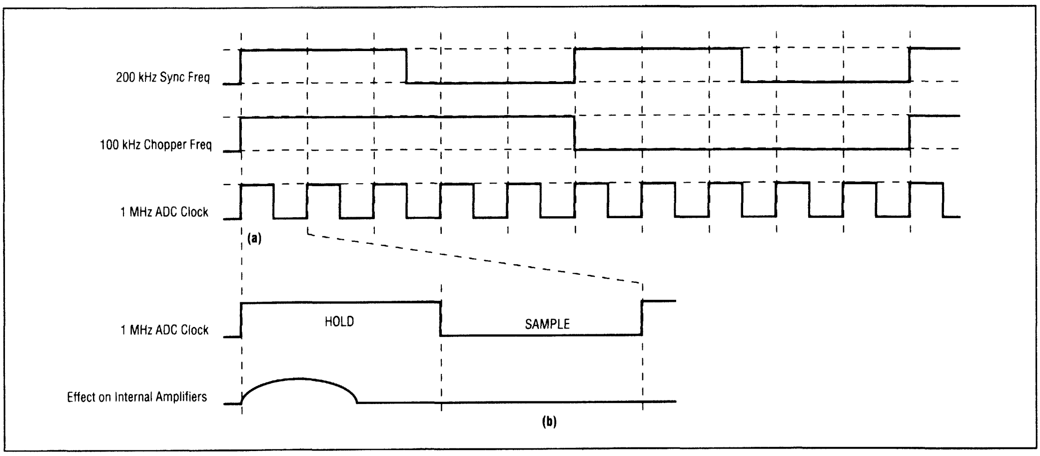


Figure 3. The ADC clock edge that puts the sample-and-hold amplifier into HOLD must be synchronized to the rising edge of the 200 kHz Sync Input (a). Any perturbation caused by the 100 kHz chopper frequency settles out prior to the next sample (b).

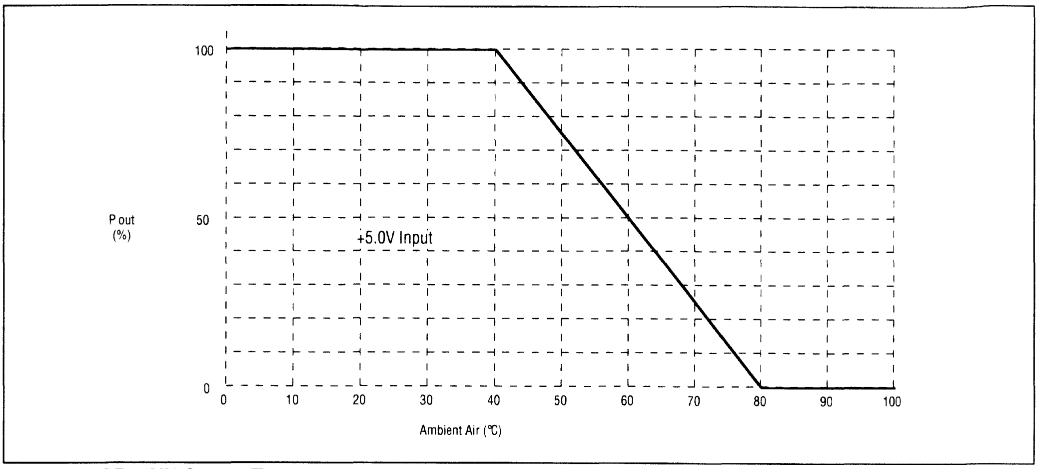


Figure 4. SP70XX Series Temperature/Power Derating Curve.

Ordering Guide

Specify:

6W @ ±15V, +5V, –6V	**SP7005**
6W @ ±15V, 5V, –5V	**SP7008**
6.75V @ ±15V, +5V	**SP7015**

SP7005/SP7008/
SP7015

Low Noise DC-to-DC Converters

for Today's State-of-the-Art Data Acquisition Systems

Introduction

The SP7005, SP7008, and SP7015 are tightly regulated, highly isolated, multiple output DC-to-DC converters. Designed specifically for the demanding performance of today's state-of-the-art data acquisition systems, this series offers exceptionally low noise, ±15V analog supplies, and a +5V supply generated from a +5V input. The SP7005 and the SP7008 offer additional –6V and –5V supplies respectively. Both the SP7005 and the SP7008 will generate 6 watts of power, while the SP7015 can generate 6.75 watts.

This series of DC-to-DC converters features low noise in both the analog and digital supplies, 5 mV p-p analog, and 10 mV p-p digital (noise plus ripple), in a 5 MHz bandwidth under full load with a line and load regulation of ±0.2%. Packaged in 1" x 3" x 0.5" fully shielded module, they have an input to output isolation of 10 MΩ and 500V RMS. Also featured is an optional sync input available to blank switching during the period of A/D conversion.

In a high performance data acquisition system, the use of linear supplies is still highly recommended. However, if the only available source of power is +5V, the SP70XX series of DC-to-DC converters offer the best possible solution.

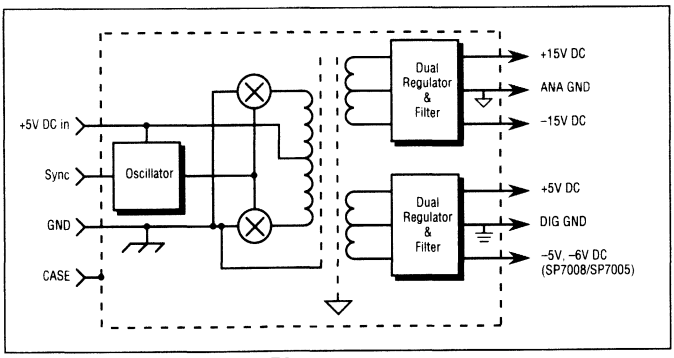


Figure 1. Functional Block Diagram

Features

- ❑ Low Noise–
  5 mV p-p Noise Plus Ripple
- ❑ ±0.2% Line Regulation
- ❑ ±0.2% Load Regulation
- ❑ Compact Size – 1" x 3" x 0.5"
- ❑ Synchronized Chopper
- ❑ 500V Input to Output Isolation

Applications

- ❑ A/D, D/A Converters
- ❑ Mixed Signal Circuits
- ❑ General Purpose Supply
- ❑ Telecommunications

SP7005/SP7008/ SP7015

Specifications[1]

	SP7005	SP7008	SP7015
ABSOLUTE MAXIMUM RATINGS (WITHOUT DAMAGE)			
Specified Temperature	0°C to +60°C	0°C to +60°C	0°C to +60°C
Operating Temperature	0°C to +60°C	0°C to +60°C	0°C to +60°C
Storage Temperature	–25°C t0 +85°C	–25°C t0 +85°C	–25°C t0 +85°C
Input Voltage	0V to +7.5V	0V to +7.5V	0V to +7.5V
Sync Input Voltage	0V to +15V	0V to +15V	0V to +15V
INPUT			
Voltage (Full Power)	5V DC ±0.25V	5V DC ±0.25V	5V DC ±0.25V
(50% Power)	5V DC ±0.5V	5V DC ±0.5V	5V DC ±0.5V
Current @ Full Load and +5.0V	1.84 A Max.	1.84 A Max.	2.05 A Max.
Reflected Input Ripple Current @ Full Load	200 mA p-p Max.	200 mA p-p Max.	170 mA p-p Max.
Sync (Negative Edge Triggered)			
Level	3.0V p-p Min.	3.0V p-p Min.	3.0V p-p Min.
Loading (Series Cap.)	4700 pF Typ.	4700 pF Typ.	4700 pF Typ.
(Series Resistor)	4.7 kΩ Typ.	4.7 kΩ Typ.	4.7 kΩ Typ.
Pulse Width	0.1 μs to 2 μs	0.1 μs to 2 μs	0.1 μs to 2 μs
Fall Time	200 ns Max.	200 ns Max.	200 ns Max.
OUTPUTS			
Voltages			
+Vcc	+15V ±0.4V	+15V ±0.4V	+15V ±0.4V
–Vcc	–15V ±0.4V	–15V ±0.4V	–15V ±0.4V
+Vdd	+5V ±0.15V	+5V ±0.15V	+5V ±0.15V
–Vdd	–6V ±0.3V	–5V ±0.25V	N/A
Currents[2]			
+Vcc	150 mA	150 mA	175 mA
–Vcc	150 mA	150 mA	185 mA
+Vdd	120 mA	120 mA	270 mA
–Vdd	150 mA	150 mA	N/A
Load Capacitance	No Maximum	No Maximum	No Maximum
Line Regulation[3]	±0.2% Max.	±0.2% Max.	±0.4% Max.
Load Regulation (All Supplies to Full Load)	±0.2% Max.	±0.2% Max.	±0.4% Max.
Temperature Coefficient	1 mV/°C	1 mV/°C	1 mV/°C
Load Transient Response to 1.0%	20 μs Max.	20 μs Max.	20 μs Max.
Noise Plus Ripple @ 5 MHz B.W.			
±Vcc	5 mV p-p Max.	5 mV p-p Max.	5 mV p-p Max.
±Vdd	10 mV p-p Max.	10 mV p-p Max.	15 mV p-p Max.
Short Circuit Protection[4]	Limits to 1.5A	Limits to 1.5A	Limits to 1.5A
CONVERSION			
Efficiency @ Full Load			
+5.25V Input	62% Typ.	62% Typ.	63% Typ.
+5.0V Input	67% Typ.	67% Typ.	66% Typ.
+4.75V Input	72% Typ.	72% Typ.	69% Typ.
Chopper Frequency			
Free Run[5]	100 kHz ±15 kHz	100 kHz ±15 kHz	100 kHz ±15 kHz
Sync Mode[6]	100 kHz ±20 kHz	100 kHz ±20 kHz	100 kHz ±20 kHz

SPECIFICATIONS	SP7005	SP7008	SP7015
ISOLATION[7]			
Resistive Coupling	10 MΩ Typ.	10 MΩ Typ.	10 MΩ Typ.
Capacitive Coupling			
(Pin 4 to Pin 11)	50 pF Typ.	50 pF Typ.	60 pF Typ.
(Pin 4 to Pin 14)	50 pF Typ.	50 pF Typ.	40 pF Typ.
(Pin 11 to Pin 14)	100 pF Typ.	100 pF Typ.	75 pF Typ.
Breakdown Voltage			
(Pin 4 to Pin 11)	500V Min.	500V Min.	500V Min.
(Pin 4 to Pin 14)	500V Min.	500V Min.	500V Min.
(Pin 11 to Pin 14)	300V Min.	300V Min.	500V Min.
Module Shielding[8]			
Electromagnetic	5 Sides	5 Sides	5 Sides
Electrostatic	6 Sides	6 Sides	6 Sides
ENVIRONMENTAL & MECHANICAL			
Operating Temperature	0°C to +50°C	0°C to +50°C	0°C to +50°C
Specified Temperature	0°C to +50°C	0°C to +50°C	0°C to +50°C
Storage Temperature	–25°C to +85°C	–25°C to +85°C	–25°C to +85°C
Case Temperature Rise[9] **@ Full Load Out and +5.0V DC In**	50°C Typ.	50°C Typ.	50°C Typ.
Relative Humidity **(Noncondensing to +50°C)**	90%	90%	90%
MTBF Prediction[10]	206048 Hrs.	206048 Hrs.	206048 Hrs.
Max. Size (Inches)	1 x 3 x 0.5	1 x 3 x 0.5	1 x 3 x 0.5
(Millimeters)	25.4 x 76.2 x 12.7	25.4 x 76.2 x 12.7	25.4 x 76.2 x 12.7
Case Potential[11]	Floating	Floating	Floating

NOTES

1. All specifications guaranteed at +25°C and +5.0V DC nominal input voltage unless otherwise noted.
2. When load current on any two outputs is reduced by 50%, the maximum load current on a third output can be increased by 50%.
3. Specified with input voltage of +4.75V to +5.25V DC.
4. The output regulators have internal over-current protection that limits their outputs to 1.5A. This protection, however, will not protect the input switcher from damage. An external 3.5A picofuse in series with the +5V DC input must be provided by the user.
5. Sync input must be left open when free running.
6. Syncs on negative edge and divides by two, i.e. 200 kHz sync creates a 100 kHz chopper frequency.
7. ±Vcc share a common ground that is isolated from ±Vdd ground.
8. A Faraday shield is tied to primary ground. A second Faraday shield is tied to ±Vcc ground.
9. The module requires two CFM air-flow across the top of it's case at elevated temperatures in an ambient environment of 25°C or higher. With fully loaded outputs, the case temperature can approach 80°C and pose a threat to the reliability of the unit.
10. References: MIL-HDBK-217E, NPRD-3 (RADC).
11. The case is electrically connected to Pin 4. The point in the system to which the case is electrically connected (if any) is left to the user's discretion.

Specifications subject to change without notice.

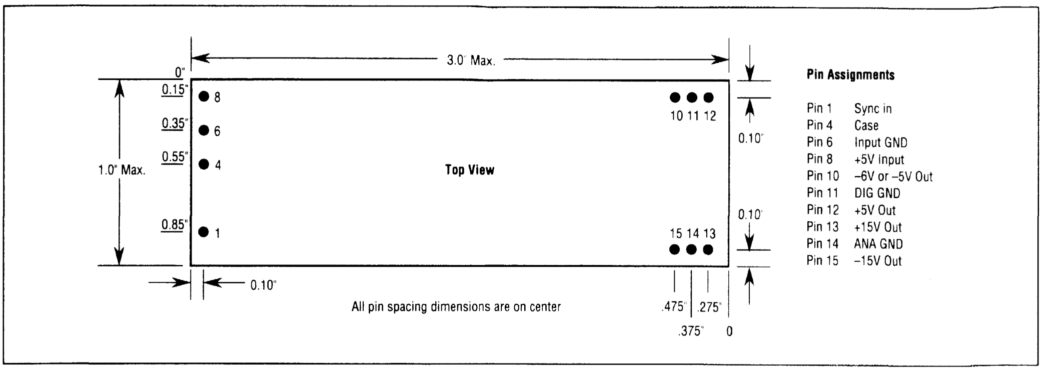


Figure 2. Mechanical and Pin Assignments.

Ordering Guide

Specify:

6W @ ±15V, +5V, –6V	**SP7005**
6W @ ±15V, +5V, –5V	**SP7008**
6.75W @ ±15V, +5V	**SP7015**

PC/AT and PC/104 Boards

Selection Guide

1 MHz Sampling Rate Data Acquisition Boards

for the PC/AT (Optional DSP Interface)

FAST12-1, FAST12-1 (SSH), FAST14-1, FAST16-1

Introduction

Analogic's FAST series of PC/AT-compatible data acquisition boards offers a wide range of capabilities for high speed/high performance applications. This versatile family is offered in 12-, 14-, and 16-bit versions with optional on-board sample memory or DSP interconnection. All the models perform to exacting specifications at a 1 MHz peak sample rate, or 250 kHz/channel across all four channels.

FAST12 (except the -4S version), FAST14, and FAST16 offer software programmable input ranges, as well as a 4-channel low-noise multiplexer, in a single PC/AT slot. In addition, an optional 8-channel sample-and-hold companion board (Model SSH-8) supports either eight or sixteen inputs of simultaneous data acquisition. On-board sample memory is available in 1, 2, 4 or 8 Megasample versions to facilitate transient data capture in real time.

A digital signal processing (DSP) interconnection is offered in either of the most popular DSP Interface Standards: DSP~Link™ or DT-Connect™. This option consists of a daughterboard that replaces the sample memory option for the FAST series and interconnects to a companion DSP board in an adjacent slot.

Continued on page 136.

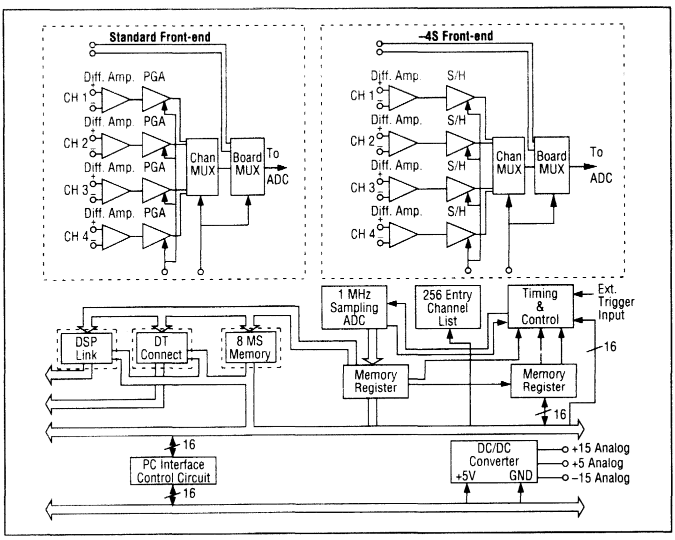
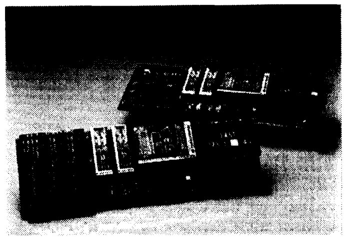


Figure 1. FAST Series Functional Block Diagram.



Features

- ❑ PC/AT-compatible
- ❑ 12-, 14- and 16-bit Resolution
- ❑ 1 MHz Sampling Rate
- ❑ Optional DSP Interface
- ❑ Four Differential Input Channels
- ❑ 4-Channel SSH Option
- ❑ Programmable Input Ranges
- ❑ Up to Eight Megasample On-board Memory
- ❑ 256-Entry Channel List
- ❑ Flexible Triggering Modes
- ❑ DMA Data Transfer
- ❑ Software Calibration
- ❑ Application Software Support

Applications

- ❑ Vibration Analysis
- ❑ Sonar
- ❑ Automatic Test Equipment
- ❑ CCD Imaging
- ❑ Waveform Analysis
- ❑ Transient Analysis
- ❑ Speech Processing
- ❑ Spectral Analysis

DSP~Link™ is a trademark of Spectrum Signal Processing, Inc.

DT-Connect™ is a trademark of Data Translation, Inc.

	FAST12-1	FAST14-1
ANALOG INPUT		
Number of Channels	Four Differential	Four Differential
Max. Input Without Damage		
Power On	±35V	±35V
Power Off	±20V	±20V
Input Voltage Ranges		
Unipolar	+2.5V, +5.0V, +10V (special order)	+2.5V, +5.0V, +10V (special order)
Bipolar	±2.5V, ±5V, ±10V	±2.5V, ±5V, ±10V
Input Bias Current	5 nA Typ.	5 nA Typ.
Input Resistance	100 MΩ Typ.	100 MΩ Typ.
Input Capacitance	50 pF Typ.	50 pF Typ.
Common Mode Rejection	80 dB Min. DC to 120 Hz	80 dB Min. DC to 120 Hz
ADC TRANSFER CHARACTERISTICS		
Resolution	12 bits	14 bits
Quantization Error	±0.5 LSB	±0.5 LSB
No Missing Codes	Guaranteed	Guaranteed
Relative Accuracy	±0.012% FSR Max.	±0.006% FSR Max.
Absolute Accuracy [2]	±0.03% FSR Max.	±0.03% FSR Max.
Noise [3]	0.25 LSB RMS Max.	0.7 LSB RMS Max.
ADC DYNAMIC CHARACTERISTICS		
Maximum Sampling Rate	1 MHz Min.	1 MHz Min.
Crosstalk [4]	–90 dB Max.	–90 dB Max.
S/H Feedthrough	–84 dB Max.	–84 dB Max.
Channel/Channel Timing Skew	N/A	N/A
Signal to Noise Ratio [5]	72 dB Min.	73 dB Min.
Peak Distortion [6]	–75 dB Max.	–78 dB Max.
Total Harmonic Distortion [7]	–72 dB Max.	–76 dB Max.
Full Power Bandwidth	500 kHz Typ.	500 kHz Typ.
Slew Rate	32 V/µs	32 V/µs
Settling Error at Max. Rate	.02% of 1/2 FSR	.02% of 1/2 FSR
STABILITY		
Offset Tempco	±200 µV/°C Max.	±150 µV/°C Max.
Gain Tempco	±50 ppm/°C Max.	±35 ppm/°C Max.
Differential Linearity TC	±2 ppm/°C Max.	±1 ppm/°C Max.
Reference TC	±5 ppm/°C Typ.	±5 ppm/°C Typ.
Warm-Up Time	10 Minutes	10 Minutes
TRIGGER		
Trigger Modes Programmable	Host Software	Host Software
16 – 32 Bit Counter	Internal	Internal
External	TTL, Positive/Negative Slope	TTL, Positive/Negative Slope
Analog (Memory Options Only)	Level or slope, 8-bit Resolution	Level or slope, 8-bit Resolution
External Trigger Loading	1 TTL Load	1 TTL Load
External Minimum Pulse Width	200 ns	200 ns
TIME BASE		
Sampling Period	1 µs to 7 Min. in 100 ns Increments	1 µs to 7 Min. in 100 ns Increments
Time Base Delay (Memory Options Only)	100% Pre-trigger to 100% Post-trigger	100% Pre-trigger to 100% Post-trigger
ENVIRONMENTAL		
PC/AT Bus Required Voltage	+5V ±5%	+5V ±5%
Current	6A Max.	6A Max.
Power Consumption	30W Max.	30W Max.
Operating Temperature	+5°C to +50°C	+5°C to +50°C
Storage Temperature	–25°C to +85°C	–25°C to +85°C
Relative Humidity	40%, Noncondensing to +50°C	40%, Noncondensing to +50°C
Mounting Bracket Potential	Ground	Ground
Physical Size	Full Size, Single slot PC/AT Card	Full Size, Single slot PC/AT Card
RFI/EMI Compatibility	Guaranteed	Guaranteed

	FAST16-1	FAST12-1 (SSH)
ANALOG INPUT		
Number of Channels	Four Differential	Four Differential (SSH)
Max. Input Without Damage		
Power On	±35V	±35V
Power Off	±20V	±20V
Input Voltage Ranges		
Unipolar	+2.5V, +5.0V, +10V	+10V
Bipolar	±2.5V, ±5V, ±10V	±5V
Input Bias Current	5 nA Typ.	5 nA Typ.
Input Resistance	100 MΩ Typ.	100 MΩ Typ.
Input Capacitance	50 pF Typ.	50 pF Typ.
Common Mode Rejection	80 dB Min. DC to 120 Hz	72 dB Min. DC to 120 Hz
ADC TRANSFER CHARACTERISTICS		
Resolution	16 bits	12bits
Quantization Error	±0.5 LSB	±0.5 LSB
No Missing Codes	Guaranteed	Guaranteed
Relative Accuracy	±0.003% FSR Max.	±0.012% FSR Max.
Absolute Accuracy [2]	±0.012% FSR Max.	±0.03% FSR Max.
Noise [3]	1.0 LSB RMS Max.	0.25 LSB RMS Max.
ADC DYNAMIC CHARACTERISTICS		
Maximum Sampling Rate	1 MHz Min.	1 MHz Min.
Crosstalk [4]	–90 dB Max.	–90 dB Max.
S/H Feedthrough	–84 dB Max.	–84 dB Max.
Channel/Channel Timing Skew	N/A	±2.5 ns Max.
Signal to Noise Ratio [5]	84 dB Min.	72 dB Min.
Peak Distortion [6]	–90 dB Max.	–75 dB Max.
Total Harmonic Distortion [7]	–88 dB Max.	–72 dB Max.
Full Power Bandwidth	500 kHz Typ.	500 kHz Typ.
Slew Rate	32 V/µs	32 V/µs
Settling Error at Max. Rate	.02% of 1/2 FSR	.02% of 1/2 FSR
STABILITY		
Offset Tempco	±100 µV/°C Max.	±200 µV/°C Max.
Gain Tempco	±20 ppm/°C Max.	±50 ppm/°C Max.
Differential Linearity TC	±1 ppm/°C Max.	±2 ppm/°C Max.
Reference TC	±5 ppm/°C Typ.	±5 ppm/°C Typ.
Warm-Up Time	10 Minutes	10 Minutes
TRIGGER		
Trigger Modes Programmable	Host Software	Host Software
16 – 32 Bit Counter	Internal	Internal
External	TTL, Positive/Negative Slope	TTL, Positive/Negative Slope
Analog (Memory Options Only)	Level or slope, 8-bit Resolution	Level or slope, 8-bit Resolution
External Trigger Loading	1 TTL Load	1 TTL Load
External Minimum Pulse Width	200 ns	200 ns
TIME BASE		
Sampling Period	1 µs to 7 Min. in 100 ns Increments	1 µs to 7 Min. in 100 ns Increments
Time Base Delay (Memory Options Only)	100% Pre-trigger to 100% Post-trigger	100% Pre-trigger to 100% Post-trigger
ENVIRONMENTAL		
PC/AT Bus Required Voltage	+5V ±5%	+5V ±5%
Current	6A Max.	6A Max.
Power Consumption	30W Max.	30W Max.
Operating Temperature	+5°C to +50°C	+5°C to +50°C
Storage Temperature	–25°C to +85°C	–25°C to +85°C
Relative Humidity	40%, Noncondensing to +50°C	40%, Noncondensing to +50°C
Mounting Bracket Potential	Ground	Ground
Physical Size	Full Size, Single Slot PC/AT Card	Full Size, Single Slot PC/AT Card
RFI/EMI Compatibility	Guaranteed	Guaranteed

NOTES:

1. Unless otherwise noted, all specifications apply at +25°C and power supply at +5.0V.
2. Referred to on-board reference. Absolute accuracy before calibration is –0.7% to ±0.2% FSR maximum.
3. Combined thermal noise of input amplifier, S/H amplifier, and ADC noise, not including quantization noise. Referred to ±5V voltage range.
4. Measured with a ±5V sinusoidal 20 kHz input signal.
5. Signal-to-Noise Ratio represents the logarithmic ratio between the RMS value of the signal and the total RMS noise below the Nyquist rate. The total RMS noise is computed by: (1) summing the noise power in all frequency bins not correlated with the test signal; (2) estimating the total noise power contained in all harmonically related frequency bins; and (3) computing the RMS noise from the sum of (1) and (2), measured with a ±5V 20 kHz input signal.
6. Peak Distortion represents the logarithmic ratio between the highest spurious frequency component below the Nyquist rate and the input signal. Note that in computing peak distortion, the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed (see Note 5). Measured with a ±5V 20 kHz input signal.
7. Total Harmonic Distortion represents the logarithmic ratio between the RMS sum of all harmonics up to the 100th harmonic and the RMS value of the input signal. Note that in computing THD, the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed (see Note 5). Measured with a ±5V 20 kHz input signal.

Specifications subject to change without notice.

Continued from page 133.

The FAST12-1-n-4S provides the capability to sample four channels simultaneously (SSH), and convert with 12-bit resolution, at a 250 kHz/channel rate. A single input can be sampled at 1 MHz. It offers a cost-effective and efficient solution for many applications.

Software support is provided in the form of routines to run, test, and set up the hardware functions on the board. In addition, C language libraries (Microsoft and Borland) are available to facilitate the rapid inclusion of these boards in specific applications.

HARDWARE DESCRIPTION

Analog Input Section (standard)

Each differential analog input to the FAST Series contains a multiplexer that, under software control, switches from the input signal to a reference, determined by the range of the channel, for auto-calibration. The input buffers consist of a pair of high input impedance, low bias current amplifiers. Each buffer drives one side of a well balanced differential amplifier, which then drives a programmable gain amplifier (PGA) that, under software control, sets the range of the channel. Both the differential amplifier and PGA have been carefully designed for low-noise and fast settling characteristics. The outputs of the PGAs drive a 4:1 high-speed channel select multiplexer. This is followed by a high-speed buffer amplifier that drives a 3:1 board select multiplexer that allows switching between the Master board (FAST front end) and two slave boards (SSH-8).

The board select multiplexer is connected to the input of a two-pass, sub-ranging sampling A/D converter. State-of-the-art 1 MHz, 12-, 14- or 16-bit converters with a proven track record of high reliability were chosen to provide the high performance the FAST Series requires.

Analog Input Section (SSH version)

FAST 12-1-1-4S provides a 4-channel simultaneous sample-and-hold (SSH) on the board. This feature supports sampling of very high speed signals at 1 MHz for one channel or 250 kHz/channel for four channels.

Channel List

Complex channel sequencing is simplified by use of a unique Channel List stored in on-board RAM. This list is a 256-channel entry that specifies the sequence in which input channels are to be sampled. The list, from 1 to 256 valid entries, is advanced by the internally generated ADC sampling signal at a maximum rate of 1 MHz. An entry includes: CHANNEL CODE; NULL BIT; SSH BIT; and RECYCLE BIT.

CHANNEL CODE: Indicates next channel to be sampled.

NULL BIT: A logic "1" indicates a nonconversion or "dead time" at this point in the sequence.

SSH BIT: A logic "1" indicates that this channel and the next channel will be sampled at the ADC sampling signal rate. A logic "0" indicates that this is the last channel to be sampled. The next channel will wait for a pacing signal before sampling begins. When used with a S/H slave board, the SSH BIT has a second function. A logic "1" tells the slave board to remain in HOLD. The next channel will be converted at the maximum rate. A logic "0" tells the slave to go into SAMPLE and begin acquiring new data at the completion of this channel's conversion.

RECYCLE BIT: A logic "1" indicates the last channel in the cycle. Following this last conversion, the Channel List will be recycled to the beginning at entry #0. If the SSH BIT is set to "1", the Channel List will be sequenced, again, from entry #0. If the SSH BIT is set to "0" with a logic "1" RECYCLE BIT, the converter will wait for the next Trigger and/or Pacing Signal, depending on the mode of operation.

Control Signals

The FAST Series offers three first trigger options and four second trigger options. First Trigger is used (1) to initiate a conversion sequence; and (2) as an enable (depending on the mode of operation selected). The first trigger can be selected to be an external TTL input, on-board 16- or 32-bit timer, or a programmable software bit. For all modes of operation, the first trigger initiates a conversion sequence; i.e., samples will be converted when the first trigger occurs. Subsequent conversions depend on the mode selected.

The second trigger is used to signal the end of the conversion sequence (see FREE RUN and GATED MODE). It has four available options, the three mentioned for the first trigger, and an analog voltage (available with memory options only) from one of the four input channels.

Pacing is used to initiate conversions in modes of operation where the trigger is used as a gate.

Modes of Operation

The FAST Series boards may interface to the PC/AT as a programmed I/O device or via Direct Memory Access (DMA). They offer four modes of operation for data acquisition: Normal Trigger Mode; Scan Count Mode; Free Run Mode; and Gated Mode.

NORMAL MODE: Acquisition and conversion are controlled and paced by trigger only.

SCAN COUNT MODE: This is the only mode using the Scan Counter. The Scan Counter is programmable from 1 to 255 scans through the channel list. Acquisition and conversion are controlled by the pacing signal after it has been enabled by a trigger signal. As previously stated, the first trigger initiates the first set of conversions determined by the channel list. All subsequent conversions are governed by the pacing signal and the channel list. Conversions continue, initiated by the pacing signal, until the Scan Counter is decremented to "0" or until the on-board memory generates a "Memory Full" signal.

In both Normal Trigger Mode and Scan Count Mode, after two samples are collected, a "data ready" signal will be generated, and data stored in on-board memory can be transferred to the PC via PIO or DMA. Data can be transferred "on the fly" as it is acquired, or the memory could be programmed not to transfer data until memory is full, or after a specific number of samples has been taken.

FREE RUN MODE: Again, the trigger signal is the enable with the pacing signal controlling acquisition and conversion. The first trigger starts the initial set of conversions, determined by the channel list. Subsequent conversions are governed by the pacing signal and the channel list. In the Free Run Mode, the channel listing sequence continues until the second trigger ends the sequence. At this time, a pre-programmed number of samples are taken and data can now be transferred to the PC. This mode is used to capture data around an event (pre- and post-triggered data). In this mode, data transfer to the PC is not allowed until the second trigger occurs. On-board memory is allowed to overwrite itself without an error condition.

GATED MODE: This mode of operation is the same as the Free Run Mode except that data stored in on-board memory can be transferred to the PC memory at any time, and an error condition is generated if the on-board memory overflows.

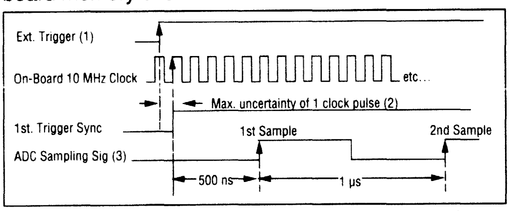


Figure 2a. Timing of External Trigger to that of On-Board Timing Signals In All Modes.

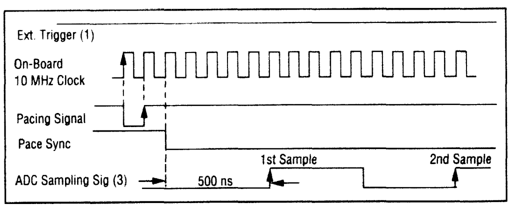


Figure 2b. Timing of On-Board Pacing Signal In the Three Paced Modes.

NOTES:

1. The external trigger can be configured in software to activate first trigger sync on either a positive or negative edge.
2. First trigger sync is generated in coincidence with rising edges of the external trigger and the on-board 10 MHz clock.
3. The ADC sampling signal, once synchronized, will initiate an ADC sample precisely every 1 µs as controlled by the channel list.

Noise Immunity

Noise immunity within the FAST Series board is achieved, maintaining true stated resolution, by use of proven high frequency layout techniques, including short leads and interconnects, guarded signal lines, and the use of separate power and ground planes within the printed circuit board's eight layers. Noise immunity is further enhanced by careful use of on-board DC-to-DC converters to generate all required supply voltages.

Typical Examples

To program FAST Series boards, both the Channel List and the selected mode of operation must be taken into consideration. Typical examples of this are described below.

Figure 3a illustrates a channel list programmed to sample all entries (eight in this example) at the full conversion rate of the A/D converter when the first pacing signal is issued. Figure 3b illustrates a channel list with an alternating SSH bit. With this channel list, channels 1 and 2 will be converted at the maximum rate of the A/D converter. The board will then wait for the next pacing signal to sample channel 3 only. On the next pacing signal, channel 2 will be sampled once; then there will be a "dead time" of one conversion period (Null Bit = "1"); then channel 3 will be sampled. Note that in the Normal mode, the first trigger becomes the pacing signal (Figures 4a and 4b); in the Scan Count Mode, the pacing signal is first gated by the first trigger (Figures 5a and 5b and Figures 6a and 6b). The examples shown are after the channel list has sequenced through at least once. For the pacing modes, the first trigger starts the conversions which continue automatically per the channel list definitions. All subsequent conversions for the paced modes are controlled by the pacing signal only.

CHANNEL LIST

Entry Number	RECYCLE Bit	SSH Bit	Null Bit	Channel
0	0	1	0	1
1	0	1	0	2
2	0	1	0	3
3	0	1	0	2
4	0	1	1	x
5	0	1	0	3
6	0	1	0	1
7	1	0	0	2
–	x	x	x	x

Figure 3a. All Channels Converted at Maximum Rate of the A/D Converter.

CHANNEL LIST

Entry Number	RECYCLE Bit	SSH Bit	Null Bit	Channel
0	0	1	0	1
1	0	0	0	2
2	0	0	0	3
3	0	1	0	2
4	0	1	1	x
5	0	0	0	3
6	0	1	0	1
7	1	0	0	2
–	x	x	x	x

Figure 3b. Alternate SSH bit. An entry following a logic "0" SSH bit must wait for a pacing signal before a conversion will take place.

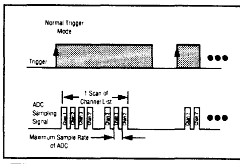


Figure 4a. Normal Mode with Channel List of Figure 3a.

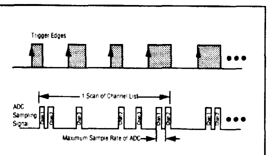


Figure 4b. Normal Mode with Channel List of Figure 3b.

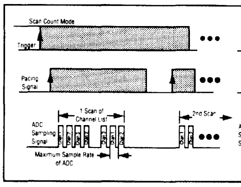


Figure 5a. Scan Count Mode with channel list of Figure 3a.

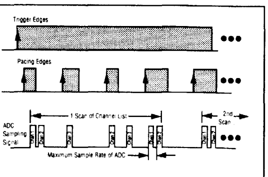


Figure 5b. Scan Count Mode with channel list of Figure 3b.

FAST SERIES PERFORMANCE TESTING

As part of our continuing effort to maintain our customers' confidence, Analogic supplies a data sheet indicating that 100% testing was performed on each device prior to shipping. Such data sheets reflect testing performed in both the "Frequency Domain" and the "Amplitude Domain."

Time Domain Testing

Time Domain Testing is performed by proprietary automatic test equipment that includes a 22-bit duty-cycle digital-to-analog converter. The data sheet provides the end customer with detailed results on integral linearity, A/D converter noise, absolute accuracy, conversion time, power supply current, and power supply rejection. Following is a list of the Analogic major definitions as tested with our "Amplitude Domain" test systems.

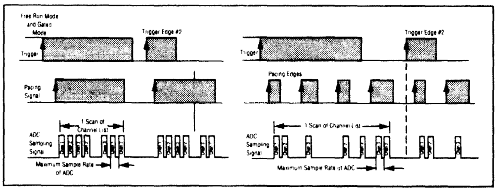


Figure 6a. Free Run or Gated Mode with Channel List of Figure 3a.

Figure 6b. Free Run or Gated Mode with Channel List of Figure 3b.

A/D CONVERTER NOISE: Errors at the output code caused by signals present other than the signal source. In FAST Series boards, this specification includes noise from the differential amplifier through and including the A/D converter.

INTEGRAL LINEARITY: A measure of the maximum deviation of the output digital codes from the best-fit straight line through the transfer function, expressed as a percentage of the full scale range. A least squares algorithm is used to determine best fit.

DIFFERENTIAL LINEARITY: A measure of the maximum deviation of any particular code width from the ideal code width, expressed as a fraction of an LSB.

$$\text{Differential Linearity} = \left| \frac{V_{MAX} - V_{LSB}}{V_{LSB}} \right| \text{LSBs}$$

where: V_{MAX} = maximum (or minimum) code width

ABSOLUTE ACCURACY: A measure of the largest static difference between the actual output code and that predicted by the ideal transfer function; a worst case summation of all error sources, expressed as a percentage of full scale.

Absolute Accuracy measurements must be referenced to a standard traceable to the NIST with at least an order of magnitude more accurate than the unit under test.

A/D CONVERSION TIME: Time measured from the rising edge of EOC (the time when the S/H goes into hold) to the falling edge of EOC. The maximum limit is based on allowing sampling rates up to 1 MHz, including a S/H.

Frequency Domain Testing

Frequency Domain Testing is performed within the PC environment. The power of the processor provides us with a great deal of flexibility in both gathering and formatting the data. While a Rosenfeld window is applied on a standard basis, other types of windows (such as Blackman-Harris and Blackman) are available for custom testing. The number of samples can be varied from 512 to 8192, and the system can average up to 64 FFTs. A typical data sheet depicting testing over frequency is shown in Figure 7.

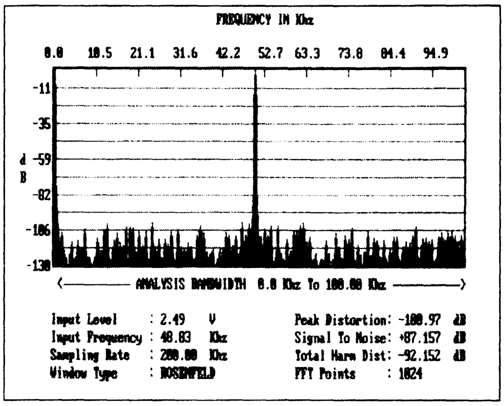


Figure 7. "Frequency Domain" Data Sheet

Memory

The optional on-board memory, based on the conversion mode of operation chosen, can be used as either a circular buffer or a single-sweep first-in-first-out (FIFO).

In the Free Run Mode, following a gated pacing signal, data will continuously be written to on-board memory, looping around from the bottom to top and writing over the original data until a second trigger occurs. As previously discussed, a pre-programmed number of samples will be taken at this point.

In all other conversion modes, the memory takes on the function of a large FIFO memory device. As data fills the FIFO, the application software can remove data on a first-in, first-out basis. If the program removes the data fast enough, the memory would never fill and data collection would continue indefinitely or as dictated by the channel list. If data is filling the memory faster than the program can transfer it to the host computer, a "memory full" signal is generated and conversion stops.

DSP Board Interface

DSP-Link and DT-Connect are external input/output data ports and software protocols that permit the direct connection of the FAST Series to processor boards for accelerated signal processing. These external ports provide direct, high-speed, 16-bit communication between the FAST Series and auxiliary boards, and can be used in either single word or block transfer mode. This set of auxiliary pathways completely eliminates host system bottlenecks. In addition, a 4K sample FIFO is included to buffer data between the two boards.

Software Description

A user-friendly Setup Program is provided with each FAST Series board. This program allows the end-user to interactively specify the following operational board parameters:

Board Select (Master or SSH-8 board)	DMA Channel
Interrupt Level	Conversion Mode
Trigger Source	Channel Listing
Analog Input Voltage Range	ADC Sampling
Number of Data Points	Rate

The board parameters selected in the Setup program are saved in a configuration file named "FAST_CFG.CFG". This configuration file may then be used to initialize the board from an application program containing the FAST library functions.

High Level Language libraries are available for custom application programming in addition to setup, demonstration, and diagnostic programs, which support all hardware functions of the FAST Series. The high-level language interface for the Analogic FAST Series simplifies programming in any of the following languages:

Microsoft C 5.1 or later.

Borland C

Ordering Guide

Specify: *FAST* __ - __ - __ - __

12—12-Bit Resolution
14—14-Bit Resolution
16—16-Bit Resolution
1—1 MHz Sample Rate
1—1 Megasample On-board Memory
2—2 Megasamples On-board Memory
4—4 Megasamples On-board Memory
8—8 Megasamples On-board memory
D—DT-Connect
L—DSP-Link
4S–Simultaneous Sample & Hold
(12-bit Versions Only)

High Speed, High Precision 16-Bit Data Acquisition Boards

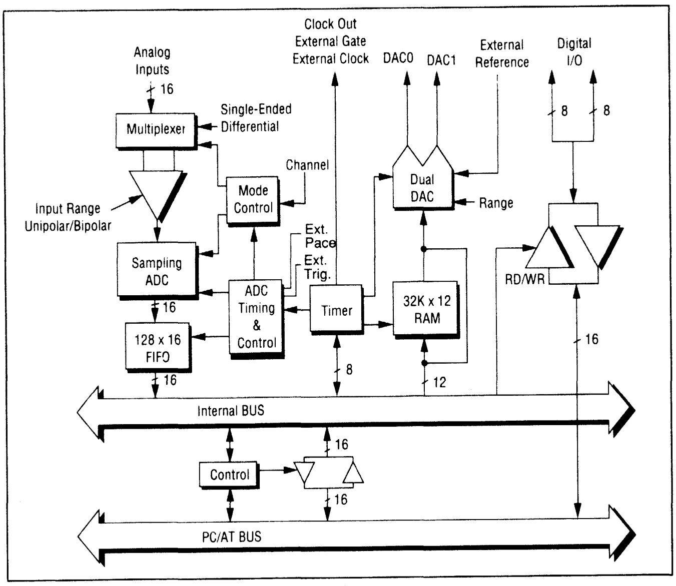
200 kHz HSDAS-16, 50 kHz LSDAS-16 for the IBM PC/AT

Introduction

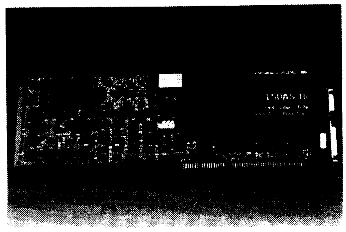
The Analogic DAS-16 Series is a high speed, high precision multifunction plug-in board for the IBM PC/AT and compatibles. These products feature a 16-input, autocalibrating analog-to-digital converter (ADC) capable of acquiring up to 200,000 samples/second. These boards also offer two low-noise, low distortion, deglitched, autocalibrating 12-bit digital-to-analog converters (DACs) with optional buffer memory. A 6-channel timer/counter and a 16-bit parallel digital input/output port are included to simplify data collection and provide external control. All functions are contained on a single-slot PC/AT compatible board, making these products the perfect choice for high performance PC-based instrumentation workstations.

The two members of the DAS-16 Series offer a selection of analog input modes and ranges not commonly available. The board may be programmed to accept single-ended or differential inputs, and one of six unipolar or bipolar full scale input ranges may be selected, all under software control. Low specified noise levels are maintained by combining skilled circuit design and multilayer circuit boards.

Extensive software libraries are available to facilitate program development. A full-function setup program and data acquisition utilities are provided. High Level Language interfaces support Microsoft C, and Borland C. Extensive user documentation is provided.



DAS-16 Series Functional Block Diagram.



Features

- ❑ 16 Single-Ended/8 Differential Inputs (expandable to 256)
- ❑ Programmable Analog Input Ranges
- ❑ 16-Bit Autocalibrating Sampling ADC
- ❑ 200 kHz ADC Sample Rate (HSDAS-16)
- ❑ Flexible Analog Triggering
- ❑ Dual 12-Bit Analog Outputs
- ❑ 32K-Sample DAC RAM
- ❑ Flexible 16-Bit Digital I/O port
- ❑ Six 16-Bit Counter/Timers
- ❑ High Speed DMA Operation
- ❑ Setup Routines and Data Acquisition Utilities Included
- ❑ Software Compatibility
- ❑ Software Calibration

Applications

- ❑ Spectroscopy
- ❑ Chromatography
- ❑ Audio
- ❑ Multichannel Data Acquisition
- ❑ High Accuracy Instrumentation
- ❑ Benchtop Test Equipment

DAS-16 SERIES

Specifications[1]

ANALOG INPUTS

Number of Channels
16-single ended, 8 differential

Input Voltage Range
2.5, 5, 10 volts (unipolar)
±2.5, 5, 10 volts (bipolar)

Maximum Input Range (signal + common mode)
±11 volts

Maximum Input Voltage
±25 volts (power ON)
±12 volts (power OFF)

Input Impedance
100 MΩ, 50 pF

Input Current
100 nA maximum

Common Mode Rejection
80 dB at 60 Hz

ANALOG INPUT ACCURACY

Resolution
16 bits

Integral Nonlinearity
±2 LSB maximum

Relative Accuracy
±0.003% of FS maximum

Absolute Accuracy[2]
±0.015% of FS maximum– uncalibrated

Monotonicity
Guaranteed

Noise[3]
1 LSB RMS maximum

STABILITY

Gain Tempco
15 ppm/°C; full-scale voltage may be autocalibrated to on-board reference voltage

Offset Tempco
Varies from 0.2 LSB/°C on ±10V range to 1.5 LSB/°C on 0-2.5V range; may be autocalibrated

Voltage Reference Tempco
5 ppm/°C

SIGNAL DYNAMICS

ADC Throughput Rate
200 kHz (HSDAS-16)
50 kHz (LSDAS-16)

Aperture Delay
30 ns (HSDAS-16)
25 ns (LSDAS-16)

Channel Crosstalk[4]
-86 dB at 1 kHz maximum (HSDAS-16)
-82 dB at 1 kHz maximum (LSDAS-16)

Channel Feedthrough
-90 dB at 1 kHz maximum

Signal-to-Noise Ratio
88 dB (fs=1 kHz, fclk=50 kHz) minimum

Total Harmonic Distortion
-90 dB (fs=1 kHz, fclk=maximum rate) maximum

Settling Error[5]
±0.005% FSR, Max.

ANALOG OUTPUTS

DAC Throughput Rate
200 kHz/channel
(software or DMA update)

Number of Channels
2

Resolution
12 bits

Output Voltage Ranges (jumper selectable)
5, 10V (unipolar)
±5, ±10V (bipolar)

Linearity
±1 LSB maximum

Gain Error
±2 LSB maximum

Offset Error
±1 LSB maximum

Settling Time to 0.01%
5 µs maximum

Slew Rate
13 V/µs

Output Current
±20 mA maximum

Glitch Energy
100 nV-second maximum

Gain Drift
±10 ppm/°C

Offset Drift
±10 ppm/°C

DIGITAL INPUT/OUTPUT

Number of Lines
16

Input Loading
1 LSTTL load

Input Pullup Resistor
10 kΩ

Output Source Current
2.6 mA minimum

Output Sink Current
24 mA minimum

COUNTER/TIMER

Timer Type
(2) Intel 82C54-2

Number of Bits
16

Reference Frequency
5.000 MHz ±0.01%

External Inputs
Gate, clock

Outputs
Pulse, square wave

ENVIRONMENTAL

Size
Full-size PC/AT

Operating Temperature
0°C to +50°C

Power Requirements
+5V ±5% @ 3A
+12V ±5% @ 500 mA
-12V ±5% @ 50 mA

RFI/EMI Compatibility
Guaranteed to preserve RFI/EMI compatibility of host IBM PC/AT

NOTES

1. Unless otherwise noted, all specifications apply at 25°C after software calibration.
2. Gain and Offset errors can be autocalibrated to within 1/2 LSB of the appropriate reference.
3. 2 LSBs max. for the 0-2.5V range.
4. The proportion of a 1 kHz signal applied to a non-selected channel input appearing on the selected channel output 20 log
5. Half-scale step on any range at the maximum sampling rate.

Specifications subject to change without notice.

Hardware Description

Each DAS-16 board consists of five interrelated subsystems: the 16-channel analog-to-digital converter (ADC); the dual digital-to-analog converter (DAC); the digital I/O port; the timer; and the PC/AT bus interface.

ANALOG-TO-DIGITAL CONVERTER: Up to sixteen single-ended or eight differential analog inputs are connected to a high speed instrumentation amplifier driving a sampling ADC. The ADC may be calibrated under software control to eliminate gain and offset errors. Data from the ADCs is buffered by a 128-sample FIFO, which allows data to be transferred from the ADC subsystem to the host PC/AT asynchronously.

The ADC subsystem operates in one of five programmable modes:

MODE 0: any one channel is sampled at maximum board speed

MODE 1: two channels are sampled at 1/2 maximum board speed

MODE 2: four channels are sampled at 1/4 maximum board speed

MODE 3: eight channels are sampled at 1/8 maximum board speed

MODE 4: all sixteen channels are sampled at 1/16 maximum board speed

Single-ended/differential mode, unipolar/bipolar mode, and input full scale range are under software control and are controlled by the software setup routines.

The ADC subsystem may be triggered by the host system or by an external signal of programmable slope and voltage level. ADC conversions may be initiated by the ADC timer, by the host, or by an external TTL signal.

DIGITAL-TO-ANALOG CONVERTERS: Two 12-bit voltage-output DACs are included to generate analog output signals, each with an integral deglitcher. Full-scale output voltage ranges are jumper-selectable, and software-controlled calibration eliminates output offset and gain errors. Each DAC subsystem includes a high speed output buffer amplifier.

An optional 32K-sample buffer memory is available for on-board waveform storage and playback.

All data transfers to the DAC are double-buffered. Data is delivered to a DAC holding register under programmed I/O from the host, under DMA, or from the optional buffer RAM. DAC clocks, which transfer data from the holding register to the DAC itself, may come from the host, from the DAC timer, or from the ADC pacing signal.

An analog comparator compares the output of either DAC with the first analog input channel to be sampled. This comparator output "tags" data from the ADC for use in pre-trigger/post-trigger applications.

DIGITAL I/O PORT: The digital I/O register can be programmed to input or output 16 bits or to output 8 bits while inputting 8 bits. All transfers are performed under software control. An external alarm input is available for handshaking and synchronization.

COUNTER/TIMER: Six 16-bit counter/timers are used. One is assigned to the ADC, one to each DAC, and two are used to clock data to/from the DAC RAM. The input and output of the sixth timer channel are available to the user for dividing an external signal, event counting, one-shot generation, and other functions of the Intel 8254 counter/timer.

CONTROL: Each DAS-16 board may interface to the PC/AT either as a programmed I/O device and/or via Direct Memory Access (DMA). As programmed I/O, the PC polls the board to determine ADC/DAC/digital I/O status or to transfer data to and/or from the board. DMA operation allows the highest speed transfers between the board and system memory. The DAS-16 DMA interface circuitry is capable of sustained transfer rates that support the maximum ADC sample rate.

Software Description

A user-friendly Setup program (MENUS) is provided with each DAS-16 board. This program allows the user to interactively specify the following operational parameters for the board:

- Single-Ended/Differential Analog Input Mode
- Analog Input Channel Selection
- Analog Input Voltage Range
- ADC Pacer Source
- ADC Sample Rate
- Number of ADC Samples to be Taken
- ADC Trigger Source
- Trigger Location within Data Buffer
- Analog Trigger Slope
- Analog Trigger Voltage

DAC Data Source
DAC Clock Source
DAC Waveform Select
DAC Waveform Characteristics

Note that each DAC may be set up independently of the other.

The board parameters selected in MENUS are saved in a configuration file named by the programmer (for example "test1.cfg"). This configuration file may then be used to initialize the board from an application program written in a high level language. The DAS-LIB High Level Language Interface for the Analogic DAS, which includes all members of the DAS-16 series, simplifies programming in any of the following languages:

Microsoft C, Borland C

Here is an example program written in Microsoft C using a configuration. file and the DAS-LIB libraries:

```
/* Initialize the driver */
bdinit(base_addr, &bd_type, adc_dma_channel,
dac_dma_channel);
/* Run the Setup program using the last configuration file */
system("menus.exe test1.cfg");
/* Set up DACs */
dainit("test1.cfg", dac_data0, dac_data1);
/* Set up ADCs */
adinit("test1.cfg");
/* Get the data */
getdma(input_data, dma_size);
/* Convert data to voltages */
for (j=0; j;j++)
  if((das_cfg_table.storage_enable>j)&1!=0)
    gtdat(input_data, j+1, volts_data, 1.0,
    WVF_LENGTH);
```

Alternatively, the DAS-LIB Interface library may be used independently of the setup program and configuration files. This library affords the programmer the opportunity to change individual board parameters independent of all other parameters.

Without a configuration file, a sample program might be structured as follows using the DAS-LIB libraries:

```
/* Initialize the board */
bdinit(base_addr, &bd_type, adc_dma_chan,
dac_dma_chan);
/* Configure DAC0 for DC, DAC1 for a waveform */
dac0setup.data = dac_data0;
dac0setup.data_buf_size = 1; /* driver uses pio */
dac1setup.data = dac_data1;
dac1setup.data_buf_size = 1024;
dac1setup.dac_rate = 50000.0;
dac1setup.update_path = 1 ;/* continuous waveform */
/* Set up DACs */
cfgdac(&dac0setup, &dac1setup);
/* Convert data to voltages */
for (j=0,j,j++)
  if(adc_gains[j]!=-1)
    gtdat(input_data, j+1, volts_data, 1.0,
    WVF_LENGTH);
```

The above code is extracted from example programs included in the High Level Language libraries for this product.

Ordering Guide

HSDAS-16	200 kHz Data Acquisition Board
LSDAS-16	50 kHz Data Acquisition Board
M Option	32 K-point Analog Output Waveform Memory

Accessories

DAS-LIB	High Level Language Libraries
ACAB-22/LN	Analog Cable with Two Connectors
DCAB-22	Digital Cable with Two Connectors
STB	Screw Terminal Breakout Box
DASMUX-64	64-Channel Multiplexer System
DASMUX-64/EX	64-Channel Expander System
MUX-16TC	16-Channel Thermocouple Multiplexer System
MUX-16TC/EX	16-Channel Thermocouple Expander System

High Speed, High Precision 12-Bit Data Acquisition Boards

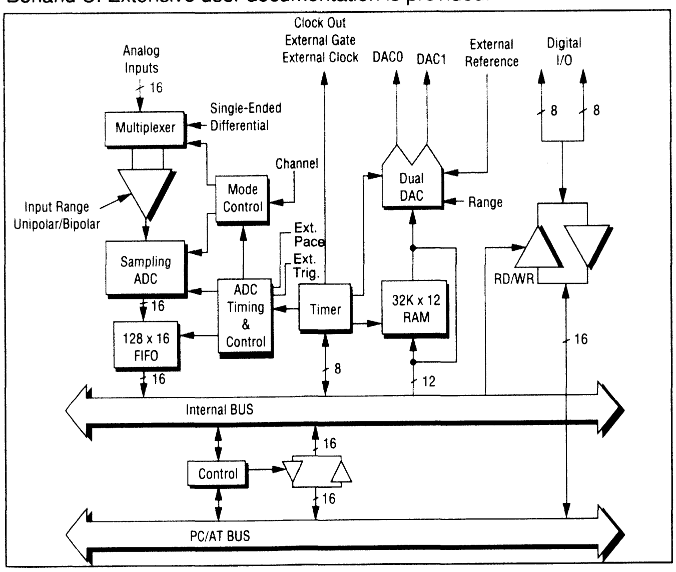
400 kHz HSDAS-12, 200 kHz MSDAS-12, 100 kHz LSDAS-12 for IBM PC/AT

Introduction

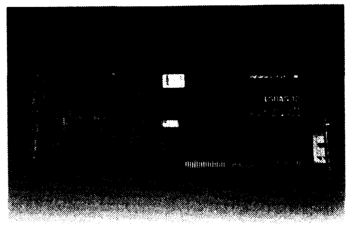
The Analogic DAS-12 Series is a family of high speed, high precision multifunction data acquisition plug-in boards for the IBM PC/AT and compatibles. These products feature a 16-input, 12-bit autocalibrating analog-to-digital converter (ADC) capable of acquiring up to 400,000 samples/second. Each board in the series also offers two low-noise, low-distortion, deglitched, autocalibrating 12-bit digital-to-analog converters (DACs) with optional buffer memory. A 6-channel timer/counter and a 16-bit parallel digital input/output port are included to simplify data collection and provide external control. All functions are contained on a single-slot PC/AT-compatible board, making these products the perfect choice for high performance PC-based instrumentation workstations.

The three members of the DAS-12 Series differ only in their ADC sample rates. The HSDAS-12 features a 400,000 samples/second ADC capable of simultaneously sampling up to four input channels. The MSDAS-12 samples at up to 200,000 samples/second and will simultaneously sample two inputs. The LSDAS-12 samples at up to 100,000 samples/second, but offers no simultaneous sampling capability.

Extensive optional software libraries are available to facilitate program development. A full-function setup program and data acquisition utilities are provided. The DAS-LIB library interfaces support Microsoft C, and Borland C. Extensive user documentation is provided.



DAS-12 Series Functional Block Diagram.



Features

- ❑ 16 Single-Ended/8 Differential Inputs (expandable to 256)
- ❑ Programmable Analog Input Ranges
- ❑ 12-bit Autocalibrating Sampling ADC
- ❑ 4-Channel Simultaneous Sample/Hold (HSDAS-12)
- ❑ 400 kHz ADC (HSDAS-12)
- ❑ Flexible Analog Triggering
- ❑ Dual 12-Bit Analog Outputs
- ❑ 32K-Sample DAC RAM
- ❑ Flexible 16-Bit Digital I/O port
- ❑ Counter/Timer
- ❑ High speed DMA Operation
- ❑ Setup Routines and Data Acquisition utilities included
- ❑ Software Compatibility
- ❑ Software Calibration

Applications

- ❑ Multichannel Data Acquisition
- ❑ Simultaneous Event Analysis
- ❑ High Speed Instrumentation
- ❑ Benchtop Test Equipment

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ANALOGIC®
The World Resource for Precision Signal Technology

DAS-12 SERIES

Specifications[1]

ANALOG INPUTS

Number of Channels
16-single ended, 8 differential

Input Voltage Range
2.5, 5, 10 volts (unipolar)
±2.5, 5, 10 volts (bipolar)

Maximum Input Range (signal + common mode)
±11 volts

Maximum Input Voltage
±35 volts (power ON)
±20 volts (power OFF)

Input Impedance
100 MΩ, 50 pF

Input Current
100 nA maximum

Common Mode Rejection
80 dB at 60 Hz

ANALOG INPUT ACCURACY

Resolution
12 bits

Differential Nonlinearity
±1 LSB maximum

Integral Nonlinearity
±1 LSB maximum

Relative Accuracy
±0.03% of FS maximum

Absolute Accuracy[2]
±0.1% of FS maximum– uncalibrated

Monotonicity
Guaranteed

Noise
1/2 LSB RMS maximum

STABILITY

Gain Tempco
20 ppm/°C; full-scale voltage may be autocalibrated to on-board reference voltage

Offset Tempco
1/4 LSB/°C; may be autocalibrated

Voltage Reference Tempco
20 ppm/°C

SIGNAL DYNAMICS

ADC Throughput Rate
400 kHz (HSDAS-12)
200 kHz (MSDAS-12)
100 kHz (LSDAS-12)

Simultaneous Sampling
4 channels (HSDAS-12)
2 channels (MSDAS-12)

Aperture Delay
25 ns

Channel Crosstalk
-70 dB at 1 kHz maximum

Channel Feedthrough
-80 dB at 1 kHz maximum

Signal-to-Noise Ratio
70 dB (fs=1 kHz, fclk=maximum rate) minimum

Total Harmonic Distortion
-72 dB (fs=1 kHz, fclk=maximum rate) maximum

ANALOG OUTPUTS

DAC Throughput Rate
200 kHz/channel
(software or DMA update)

Number of Channels
2

Resolution
12 bits

Output Voltage Ranges (jumper selectable)
5, 10V (unipolar)
±5, ±10V (bipolar)

Linearity
±1 LSB maximum

Gain Error
±2 LSB maximum

Offset Error
±1 LSB maximum

Settling Time to 0.01%
5 μs maximum

Slew Rate
13 V/μs

Output Current
±20 mA maximum

Glitch Energy
100 nV-second maximum

Gain Drift
±10 ppm/°C

Offset Drift
±10 ppm/°C

DIGITAL INPUT/OUTPUT

Number of Lines
16

Input Loading
1 LSTTL load

Input Pullup Resistor
10 kΩ

Output Source Current
2.6 mA minimum

Output Sink Current
24 mA minimum

COUNTER/TIMER

Timer Type
(2) Intel 82C54-2

Number of Bits
16

Reference Frequency
6.8 MHz ±0.01%

External Inputs
Gate, clock

Outputs
Pulse, square wave

ENVIRONMENTAL

Size
Full-size PC/AT

Operating Temperature
0°C to +50°C

Power Requirements
+5V ±5% @ 3A
+12V ±5% @ 375 mA

RFI/EMI Compatibility
Guaranteed to preserve RFI/EMI compatibility of host IBM PC/AT

NOTES

1. Unless otherwise noted, all specifications apply at 25°C after software calibration.
2. Gain and Offset errors can be autocalibrated to within 1/2 LSB of the appropriate reference.

Hardware Description

Each DAS-12 board consists of five interrelated subsystems: the 16-channel analog-to-digital converter (ADC); the dual digital-to-analog converter (DAC); the digital I/O port; the timer; and the PC/AT bus interface.

Analog-to-Digital Converter: Up to sixteen single-ended or eight differential analog inputs are connected to a high speed instrumentation amplifier driving a sampling ADC. The ADC may be calibrated under software control to eliminate gain and offset errors. Data from the ADCs is buffered by a 128-sample FIFO, which allows data to be transferred from the ADC subsystem to the host PC/AT asynchronously.

The ADC subsystem operates in one of five programmable modes:

MODE 0: any one channel is sampled at the maximum board rate.

MODE 1: two channels are sampled simultaneously at one-half the maximum board rate per channel. (MS & HS only)

MODE 2: four channels are sampled simultaneously at one-fourth the maximum board rate per channel. (HS only)

MODE 3: eight channels are sampled at one-eighth the maximum board rate per channel.

MODE 4: all sixteen channels are sampled at one-sixteenth the maximum board rate per channel.

(The maximum board rate for the HSDAS-12 is 400 kHz, the MSDAS-12 is 200 kHz, and the LSDAS-12 is 100 kHz.)

Single-ended/differential mode, unipolar/bipolar mode, and input full scale range are under software control and are controlled by the software setup routines.

The ADC subsystem may be triggered by the host system or by an external signal of programmable slope and voltage level. ADC conversions may be initiated by the ADC timer, by the host, or by an external TTL signal.

DIGITAL-TO-ANALOG CONVERTERS: Two 12-bit voltage-output DACs are included to generate analog output signals, each with an integral deglitcher. Full-scale output voltage ranges are jumper-selectable, and software-controlled calibration eliminates output offset and gain errors. Each DAC subsystem includes a high speed output buffer amplifier.

An optional 32K-sample buffer memory is available for on-board waveform storage and playback.

All data transfers to the DAC are double-buffered. Data is delivered to a DAC holding register under programmed I/O from the host, under DMA, or from the optional buffer RAM. DAC clock signals, which transfer data from the holding register to the DAC itself, may come from the host, from the DAC timer, or from the ADC pacing signal.

An analog comparator compares the output of either DAC with the first analog input channel sampled. This comparator output "tags" data from the ADC for use in pre-trigger/post-trigger applications.

DIGITAL I/O PORT: The digital I/O register can be programmed to input or output 16 bits or to output 8 bits while inputting 8 bits. All transfers are performed under software control. An external alarm input is available for handshaking and synchronization.

COUNTER/TIMER: Six 16-bit counter/timers are used. One is assigned to the ADC, one to each DAC, and two are used to clock data to/from the DAC RAM. The input and output of the sixth timer channel are available to the user for dividing an external signal, event counting, one-shot generation, and other functions of the Intel 8254 counter/timer.

Control: Each DAS-12 board may interface to the PC/AT either as a programmed I/O device or via Direct Memory Access (DMA). As programmed I/O, the PC polls the board to determine ADC/DAC/digital I/O status or to transfer data to and/or from the board. DMA operation allows the highest speed transfers between the board and system memory. The DAS-12 DMA interface circuitry is capable of sustained transfer rates of up to 400,000 samples per second to the PC, thus supporting the maximum ADC sample rate, or the maximum DAC update rate.

Software Description

A user-friendly Setup program (DAS_MENU) is provided with each DAS-12 board. This program allows the user to interactively specify the following operational parameters for the board:

Single-Ended/Differential Analog Input Mode
Analog Input Channel Selection
Analog Input Voltage Range
ADC Pacer Source
ADC Sample Rate
Number of ADC Samples to be Taken
ADC Trigger Source
Trigger Location within Data Buffer
Analog Trigger Slope
Analog Trigger Voltage
DAC Data Source
DAC Clock Source
DAC Waveform Select
DAC Waveform Characteristics

Note that each DAC may be set up independently of the other.

The board parameters selected in (DAS_MENU) are saved in a configuration file named by the programmer (for example "test1.cfg"). This configuration file may then be used to initialize the board from an application program written in a high level language. The DAS library for the DAS-12 Series of Boards simplifies programming in either of the following languages:

Microsoft C
Borland C

Ordering Guide

HSDAS-12............................400 kHz Data Acquisition Board
MSDAS-12...........................200 kHz Data Acquisition Board
LSDAS-12............................100 kHz Data Acquisition Board
M Option ......32 K-point Analog Output Waveform Memory

Accessories

DAS-LIB................................High Level Language Libraries
ACAB-22/LN ....Analog Cable with Two Connectors
DCAB-22..........................Digital Cable with Two Connectors
STB ....Screw Terminal Breakout Box
DASMUX-64 ....64-Channel Multiplexer System
DASMUX-64/EX ....64-Channel Expander System
MUX-16TC...................................16-Channel Thermocouple Multiplexer System
MUX-16TC/EX.............................16-Channel Thermocouple Expander System

DAS-12/50
DAS-12/125

Low-Cost, High-Performance Data Acquisition System

for use in Computers with ISA Bus Architecture

Introduction

The Analogic DAS-12/50 and DAS-12/125 boards are low-cost, high-performance data acquisition systems for use in computers with the ISA bus architecture, including IBM PC/ATs and compatibles. Analog inputs are digitized to 12 bits at aggregate rates up to 125 kHz. These systems also include two 12-bit analog output channels with maximum update rates of 100 kHz, two 8-bit digital I/O ports for switch, relay or LED control applications; two internally and one externally available 16-bit counter/timer for event counting, rate generation, one-shot generation, and other applications. Functions are contained on a single-slot ISA bus compatible card, making the DAS-12/50 and DAS-12/125 the best values for low-cost, high- performance PC-based instrumentation and control workstations.

The DAS family offers a variety of analog input modes and ranges and many A/D pacing and triggering options. The board may be configured to accept 16 single-ended, or 8 fully differential analog input channels. These can be expanded up to 256 single-ended or 128 differential channels with the use of four external DASMUX-64s. One of five analog input ranges, along with single-channel, auto-increment, or burst pacing modes, and internal or external triggering can be selected.

Setup programs with data acquisition utilities and diagnostic programs are provided. Also supplied are High Level Language interfaces to support C and Turbo Pascal. Extensive user and reference documentation is provided.

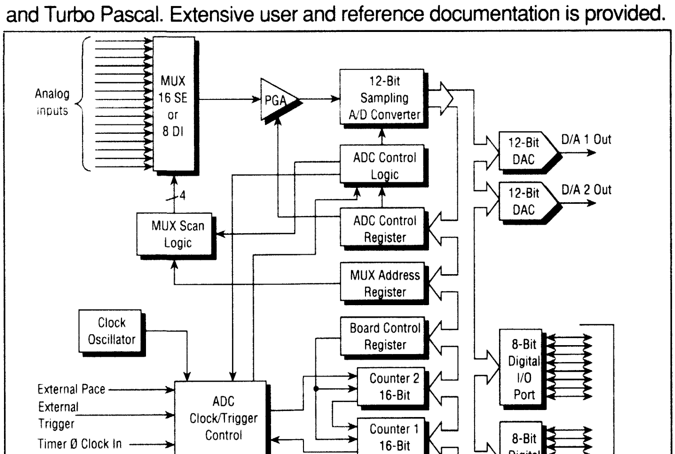
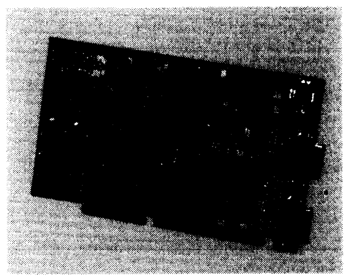


Figure 1. DAS Series Simplified Block Diagram.



Features

- ❑ 16 Single-Ended or 8 Differential Channels (Expandable to 256)
- ❑ Programmable Input Range
- ❑ 12-Bit A/D Sampling
- ❑ 125 kHz ADC Sample Rate (DAS-12/125)
- ❑ Flexible ADC Pacing and Triggering
- ❑ Dual 12-Bit Analog Outputs
- ❑ Dual 8-Bit Digital I/O Ports
- ❑ 16-Bit Counter/Timer
- ❑ High Speed DMA Operation on A/D Data
- ❑ Setup Routines, Data Acquisition Utilities, and Diagnostic Programs Provided
- ❑ Software Compatibility

Applications

- ❑ Multichannel Data Acquisition
- ❑ High Speed Instrumentation
- ❑ Benchtop Test Equipment

ANALOGIC®
The World Resource for Precision Signal Technology

DAS-12/50
DAS-12/125
Specifications[1]

ANALOG INPUT

Number of Channels
16 single-ended 8 fully differential

Input Voltage Ranges (jumper/software-selectable)
±0.625V ± 1.25V
±2.5V ± 5V ±10V

Maximum Input Voltage
±20 volts (power off)
±35 volts (power on)

Input Impedance
10MΩ // 100 pF (on channel)
10 MΩ // 10 pF (off channel)

Input Bias Current
100 nA (on channel)
10 nA (off channel)

Common Mode Input Voltage
8 volts Max.

Common Mode Rejection
70 dB Min. @ 60 Hz
(Gain = 1, RS < = 1k)

Channel Conversion Time
8 µs Max. DAS-12/125
20 µs Max. DAS-12/50

Referred Input Noise
0.4 LSB rms

ANALOG INPUT ACCURACY

Resolution
12 Bits

Offset Error
Adjustable to zero

Gain Error
Adjustable to zero

Absolute Accuracy
0.05% of FSR Max.
(PGA gain = 1)

Data Coding
Offset binary

Integral Nonlinearity
±1 LSB Max.

Differential Nonlinearity
No missing codes

Monotonicity
Guaranteed 0°C to 60°C

STABILITY

Gain Drift
30 ppm of FSR/°C

Bipolar Offset Drift
30 ppm of FSR/°C

ANALOG OUTPUTS

Data Coding
Offset binary

DAC Throughput Rate
100 kHz Max. each DAC

Settling Time to ±0.012% of FSR
10 µs

Output Range
±5 volts

Minimum Load Resistance
2K to ground

Bipolar Offset Error
±3 LSB Max.

Output Impedance
0.5Ω

Nonlinearity Error
±1 LSB Guaranteed Monotonicity

Differential Nonlinearity Error
±1 LSB Max.

Full Scale Drift
30 ppm FSR/°C

Full Scale Output Error
±0.2% of FSR Max.

DIGITAL INPUT/OUTPUT

Number of I/O Lines
(2) 8-line ports
(configurable as input or output)

Input Logic Load
1 LSTTL Load

Fanout
20 LSTTL Loads

Logic High Input Voltage
2.0 volts Min.

Logic Low Input Voltage
0.8 volts Max.

Interrupt Levels
5, 7, 10, 11, 15

DMA Channels
5, 6, 7

POWER

+5V @ ±0.25V
600 mA Typ.

+12V @ ±0.6V
40 mA Typ.

-12V @ ±0.6V
15 mA Typ.

Power
3.0W Typ.

Operating Temperature Range
0°C to 50°C

Storage Temperature Range
-25°C to 70°C

Relative Humidity
Up to 95% Non-condensing

Dimensions
7.75" W x 4.5" H x 0.062" D
(196.85 mm x 114.3 mm x 1.57 mm)

NOTE

1. Unless otherwise noted, all specifications apply at 25°C after software calibration.

HARDWARE DESCRIPTION

Each DAS board consists of four completely independent subsystems: the 16-channel analog-to-digital converter (ADC); the two 8-bit digital I/O ports; the 16-bit counters; and a dual digital-to-analog (DAC) subsystem.

Analog-to-Digital Converter

Up to sixteen single-ended or eight differential analog inputs are connected to a programmable gain amplifier which can select one gain for all input channels. This PGA drives a 12-bit sampling A/D Converter. Data from the ADC is synchronously transferred to the host computer's bus by way of polled or interrupt-driven programmed I/O, or by direct memory access (DMA). As programmed I/O, the host computer polls (or is interrupted by) the board to determine subsystem status and transfers data manually in software via "in" and "out" instructions to I/O port addresses. DMA usually allows the highest speed of data transfers between the board and memory. The DMA interface circuit is capable of sustained transfer rates to support the maximum ADC sample rate.

All DMA channel selections and interrupt levels are software-programmable. The base address is jumper-selectable.

The analog inputs can be scanned in one of three programmable modes:

MODE 0 - SINGLE CHANNEL: a single channel (software selectable) is sampled at the rate of the pacing signal.

MODE 1 - AUTO-INCREMENT: a group of channels, specified by a programmable start channel and stop channel, are sampled. Each pacing edge will cause the ADC to sample a channel, then increment the channel counter. When the stop channel is sampled, the channel counter will auto-initialize to the start channel, and the next pacing edge will cause a sample to be taken on the start channel. This process will continue until the pacing signal ceases, or the trigger is cleared.

MODE 2 - BURST: a group of channels, specified by a programmable start channel and stop channel, are sampled. Each pacing edge will cause the ADC subsystem to sample all channels from "start" to "stop" at the maximum rate of the A/D converter. When the stop channel is sampled, the channel counter will auto-initialize, and the ADC subsystem will stop until the next pacing edge; then the process will be repeated. The process will continue until the pacing signal ceases or the trigger is cleared.

The ADC subsystem may be triggered by the host system or by an external positive-going TTL edge. A/D conversions may be initiated by the host computer; by an external TTL signal; the N times M 32-bit timer; and, under a special mode, by an N times M times J 48-bit timer. N, M and J are all 16-bit values.

Digital I/O

Each digital I/O port can be programmed for byte input or output. All digital I/O transfers are performed under programmed I/O.

Counter/Timer

Three counter/timers are built into the DAS system. The first two counter/timers are cascaded together to provide the N times M 32-bit internal pacing signal. The third counter/timer is available for external use supporting all modes of the Intel 82C54. Alternatively, this counter/timer channel can be used in concert with the other two counter/timers to provide an extended divider for the internal pacing signal.

Digital-to-Analog Converter

Two 12-bit voltage output DACs are available to provide DC signals for control. The analog output value is updated immediately by the host computer writing a value to the DAC's data register.

SOFTWARE DESCRIPTION

End-User Support

A user-friendly setup program is provided with each DAS Series board. This program allows the end-user to interactively specify all operational parameters for the board including:

Analog Input Start and Stop Channels
A/D Subsystem Mode
A/D Pacing Source
A/D Pacing Rate
A/D Trigger Source
Interrupt Level and DMA Channel

Also included with each board is a group of demonstration programs that use all the salient features of the board and display measurements and the subsystem's status on the screen. A diagnostic program is also provided to interactively inform the customer about the hardware status.

Programmer Support

An extensive library of supporting functions comes with each DAS Series board. Support for Microsoft C, Borland C and Turbo Pascal is provided. Designed in a multilayer architecture, the programmer's library affords many levels of support in one streamlined package.

The three "layers" in the design are the Kernel, the File Handler, and the Analogic Software Compatibility (ASC) layers. The architecture of the entire library is based on a board image structure (BIS). This structure carries information about the hardware configuration, board identification, and information about each individual subsystem. This facilitates the use of multiple boards, running concurrently, in a single system.

The **ASC Layer** is the top level. It contains all of the subsystem-oriented functions. These include:

ASC_CreateBoardImage	Creates board image structure (BIS)
ASC_CFG_Init	Loads BIS from specified configuration file
ASC_Init	Initializes the DAS based on BIS
ASC_Report_Data	Deinterleaves multi-channel analog input data
ASC_Stop_DMA	Disables DMA requests from DAS, and disables host PC DMA controller
ASC_Status	Retrieves the DAS Status Register
ASC_Set_DMA	Sets host PC DMA controller
ASC_InstallISR	Installs an interrupt service routine by placing its address in the interrupt vector table
ASC_RemoveISR	Removes the interrupt service routine from the interrupt vector table and reinstalls the original vector
ASC_EnablePIC	Enables the PC's PIC for the specified interrupt level
ASC_DisablePIC	Disables the PC's PIC for the specified interrupt level
ASC_Serv_Intx	A simple interrupt handler
ASC_Chl_Setup	Sets start and end channels, and specifies SEQUENTIAL or BURST mode
ASC_Ch_Setup	Sets channel and SINGLE CHANNEL mode
ASC_PGA_Setup	Setup programmable gain amp. specified input range
ASC_PGA_Reset	Resets PGA to power-on condition
ASC_ADC_DMA	Enables DMA request from the DAS
ASC_ADC_Setup	Setup A/D subsystem based on BIS
ASC_DIO_Setup	Sets each 8-bit DIO port to in or out
ASC_DIO_Send	Sends specified data to DIO
ASC_DIO_Receive	Receives data from DIO
ASC_DIO_Reset	Sets both DIO ports to input and zeros the DIO data register
ASC_Pacer_SetFreq	Sets the timers to produce a specified pace frequency based on the internal pace clock frequency
ASC_Pacer_SetDiv	Loads the timers with the specified value

ASC_Load_Timer	Utility for setting a single timer on the 82C54 with specified mode and value
ASC_MUX_Chan	Returns the current MUX channel
ASC_ADC_Sample	Obtains a single sample from the A/D
ASC_DAC_Send	Sends a specified voltage to one or more DACs
ASC_DAC_Reset	Resets one or more DACs by sending the code for 0 volts to it
ASC_PaceSource	Sets the pacing source and polarity
ASC_TriggerSource	Sets the trigger source and polarity

The **Kernel Layer** is the bottom level. It contains all functions that interact directly with the DAS board and the board image structure (BIS). These functions include:

LCD_RESET	Issues a global reset and updates BIS
LCD_Activate	Sends BIS data to the DAS
LCD_Read	Retrieves all register information from the DAS and puts into BIS
LCD_Read_Status	Reads the status register of the DAS
LCD_Read_ADC	Reads a specified number of A/D data samples from the DAS (can be >64K) using A/D polling
LCD_Read_ADC_I	Reads specified number (≤64K) of samples from the A/D using A/D polling
LCD_Write_DAC	Writes a specified voltage to one or both DACs
LCD_RD_REG	Returns a 16-bit I/O port value
LCD_WR_REG	Sends a 16-bit I/O port value
LCD_Int_Master	Enables/Disables the master interrupt bit
LCD_Int_Disable	Disables one or more interrupt sources
LCD_Int_Enable	Enables one or more interrupt sources
LCD_Issue_SWPace	Issues a S/W pace signal
LCD_Clr_StatusBit	Clears and re-enables one or more status bits
LCD_Status Bit_Off	Disables one or more status bits
LCD_Timer_Int	Enables/Disables the timer interrupt
LCD_TestImage	Tests for a valid BIS
LCD_SW_TriggerBit	Sets the S/W trigger bit high or low
LCD_GO	Starts previously configured DAS
LCD_STOP	Halts the DAS board

The **File Handler Layer** stands alone. It serves the disk interaction needs of the programmer's library. These functions are:

LCD_CFG_Read	Reads a specified configuration file from disk into specified BIS
LCD_CFG_Write	Writes a specified BIS into a specified configuration file on disk

Ordering Guide

DAS-12/50	50 kHz A/D Board
DAS-12/125	125 kHz A/D Board

Accessories

ACAB-22/LN	Analog Cable with Two Connectors
DCAB-22	Digital Cable with Two Connectors
STB	Screw Terminal Breakout Box
DASMUX-64	64-Channel Multiplexer System
DASMUX-64/EX	64-Channel Expander System
MUX-16TC	16-Channel Thermocouple Multiplexer System
MUX-16TC/EX	16-Channel Thermocouple Expander System
QWIK CNT-ST	Screw Terminal Connector
QWIK CNT-RC	Ribbon Cable Connector
AC-26	26-pin Connector Kit (analog)
DC-26	26-pin Connector Kit (digital)

AIM16-1/104
AIM12-1/104

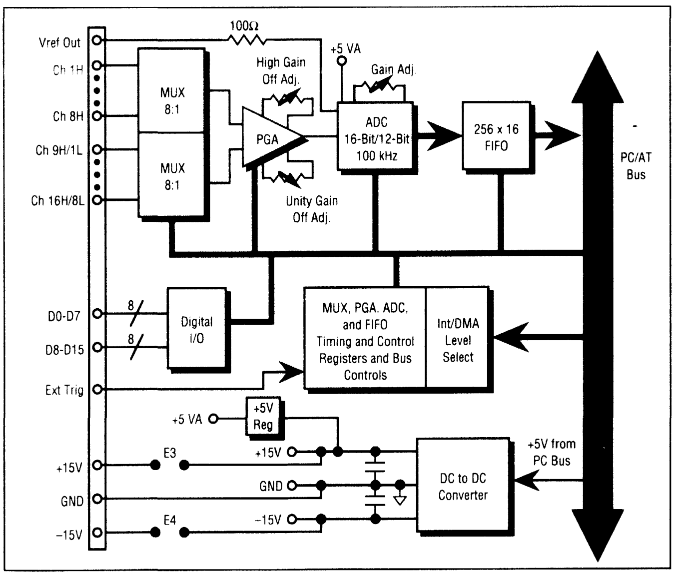
16- and 12-Bit, 16-Channel, 100 kHz PC/104 Analog Input Boards

Conform to the PC/104 Standard

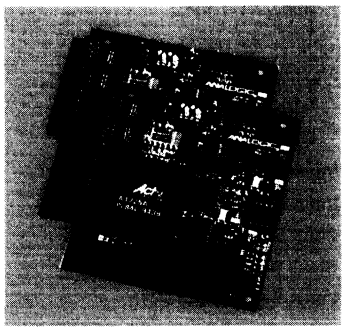
Introduction

The Analogic AIM16-1/104 and AIM12-1/104 are 16-channel, 16- and 12-bit, 100 kHz analog input boards that conform to the PC/104 standard. The AIM16/12-1/104 Series provides 16 bits of digital I/O, flexible triggering options, direct memory access (DMA), and interrupt operation. This series was designed specifically for embedded applications requiring high speed and high resolution characteristics. The analog input multiplexer is software-configurable for up to 16 single-ended or 8 differential channels, with an on-board programmable gain amplifier (PGA) providing bipolar or unipolar input ranges of 10V, 5V, 2.5V, and 1.25 V for the AIM16-1/104, and 10V, 1V, and 100 mV for the AIM12-1/104. The PGA, programmable "on the fly", drives a 16-bit or 12-bit, 100 kHz sampling ADC capable of 85 dB of spurious free dynamic range for the AIM16-1/104, and 75 dB for the AIM12-1/104. The data is first passed through a 256 x 16 bit FIFO before transferring to the host via programmed I/O or DMA in 16-bit format. The AIM16/12-1/104 series also provides 16 digital I/O bits that can be programmed as inputs and/or outputs in 8-bit bytes.

Noise immunity within the AIM16/12-1/104 series is achieved by use of proven high frequency layout techniques, including short, guarded signal paths, and use of separate power and ground planes within the printed circuit board. The use of an on-board DC-to-DC converter, powered from a single +5V supply, provides noise isolation from the system switching power supply.



AIM16/12-1/104 Functional Block Diagram



Features

- ❑ 12- or 16-Bit Resolution
- ❑ On-Board Sample and Hold Amplifier and DC/DC Converter
- ❑ 100 kHz Throughput Rate
- ❑ 8 Differential or 16 Single-ended Inputs
- ❑ Software-Selectable Input Ranges -
  AIM16-1/104:
  10V, 5V, 2.5V, and 1.25V
  AIM12-1/104:
  10V, 1V, and 100 mV
- ❑ PC/AT Stack-Through Configuration
- ❑ Operates from Single +5V Supply
- ❑ DMA and Interrupt Operation
- ❑ Flexible Triggering Capabilities
- ❑ 16 Digital I/O lines
- ❑ Conforms to PC/104 Standard

ANALOGIC

The World Resource for Precision Signal Technology

AIM16-1/104
AIM12-1/104
Specifications[1]

	AIM16-1/104	AIM12-1/104
ANALOG INPUTS (2)		
Resolution	16 Bits	12 Bits
Analog Input Voltage Range		
AIM16/12-1/104B	±1.25V, ±2.5V, ±5V, ±10V	±100 mV, ±1V, ±10V
AIM16/12-1/104U	0V to +1.25V, 0V to +2.5V, 0V to +5V, 0V to +10V	0V to +100 mV, 0V to +1V, 0V to +10V
Maximum Input Without Damage		
With power applied	±35V	±35V
With power off	±20V	±20V
Input Configuration	16 SE or 8 Diff. Channels	16 SE or 8 Diff. Channels
Input Impedance	100 MΩ//50pF Typ.	100 MΩ//50pF Typ.
Input Bias Current	100 nA Max.	100 nA Max.
Small Signal Bandwidth	1 MHz Typ.	
Large Signal Bandwidth	100 kHz Typ.	1 MHz (10V and 1V ranges) 500 kHz (100 mV ranges)
Common Mode Rejection from DC to 60 Hz with 1KΩ Source Imbalance	–80 dB Min., -100 dB Typ.	–70 dB Min., -100 dB Typ.
Integral Nonlinearity	±0.0045% Max.	±0.024% Max.
Differential Nonlinearity	±0.0045% Max.	±0.024% Max.
Monotonicity	Guaranteed	Guaranteed
Missing Codes over Specified Temperature Range	None	None
Absolute Accuracy, Software Calibration	±3 LSB	±1 LSB
Offset Error before Software Calibration	±3 mV Max.	±3 mV Max.
Offset Tempco	±150 μV/°C Max. RTO	±150 μV/°C Max. RTO
Gain Error before Software Calibration	±0.15% FSR Max.	±0.15% FSR Max.
Gain Tempco	±25 PPM/°C Max.	±25 PPM/°C Max.
Noise (RTI)		
20V p-p FSR	1.5 LSBs RMS Max.	1.0 LSB RMS Max.
10V p-p FSR	2.0 LSBs RMS Max.	N/A
5V p-p FSR	2.6 LSBs RMS Max.	N/A
2.5V p-p FSR	4.0 LSBs RMS Max.	N/A
2V p-p FSR	N/A	2.0 LSBs RMS Max.
200 mV p-p FSR	N/A	3.0 LSBs RMS Max.
Maximum Throughput Rate	100 kHz Min.	100 kHz Min
Signal to Noise Ratio 1 kHz Input @ -1 dB (3)	80 dB Min.	67 dB Min.
SFDR @ 1 kHz Input @ -1 dB (4)	85 dB Min.	75 dB Min.
THD @ 1 kHz Input @ -1 dB (5)	–80 dB Max.	–74 dB Max.
Channel-to-Channel Crosstalk	–70 dB @ 10 kHz input	–70 dB @ 10 kHz input
Step Response, Max.	±2 LSBs for 1/2 FSR Step	±2 LSBs for 1/2 FSR Step

DATA TRANSFER		
Output Coding	Offset Binary, Binary, 2's Complement	Offset Binary, Binary, 2's Complement
Transfer to Host	PI/O or DMA (3 Channels)	PI/O or DMA (3 Channels)
Interrupts	6-Level (jumper-selectable)	6-Level (jumper-selectable)
FIFO (6)	256 x 16	256 x 16
TRIGGERING OPTIONS (SOFTWARE-PROGRAMMABLE)		
External		
Polarity	Negative Slope	Negative Slope
Minimum Pulse Width	100 nS	100 nS
Loading	1 CMOS Load	1 CMOS Load
Aperture Delay (Mode 0)	40 ns	40 ns
24-Bit Counter, Internal		
Minimum Timing	10 µs	10 µs
Maximum Timing	1.67 Sec.	1.67 Sec.
Host Software	Programmable	Programmable
DIGITAL INPUT/OUTPUTS		
Compatibility	TTL, HCT, and ACT	TTL, HCT, and ACT
Number of I/O Lines (configurable as inputs or outputs)	Two 8-bit bytes	Two 8-bit bytes
Input Load	1 CMOS Load	1 CMOS Load
Fanout	±10 mA sink/source	±10 mA sink/source
Logic "0" Input	+0.8V Max.	+0.8V Max.
Logic "1" Input	+2.0V Min.	+2.0V Min.
POWER REQUIREMENTS & ENVIRONMENTAL		
+5V @ 0.5A (PC/AT bus)	±5%	±5%
Total Power Consumption	2.5W Typ.	2.5W Typ.
±15V Current Externally Available	3 mA Max.	3 mA Max.
Operating Temperature Range	+5°C to +50°C	+5°C to +50°C
Dimensions, PC/104 Stack-through Configuration	3.6" x 3.8" (91.44 mm x 96.52 mm)	3.6" x 3.8" (91.44 mm x 96.52 mm)
MTBF @ 40°C per MIL HDBK 217F	280,000 Hrs	280,000 Hrs

NOTES:

1. All specifications guaranteed at 25°C unless otherwise noted and power supply at +5.0V. Subject to change without notice.
2. All dynamic characteristics measured on the ±5V input range.
3. Signal to Noise Ratio represents the ratio, expressed in dB, between the RMS value of the signal and the total RMS noise below the Nyquist rate. Note that all frequency bins that are correlated with the test frequency are removed and replaced with an average of the remaining bins.
4. SFDR (Spurious Free Dynamic Range) represents the ratio, expressed in dB, between the RMS value of the full scale input signal and the RMS value of the highest spurious spectral component below the Nyquist rate.
5. THD (Total Harmonic Distortion) represents the ratio, expressed in dB, between the RMS sum of all harmonics up to the 100th harmonic and the RMS value of the signal.
6. For larger FIFO requirements, consult factory.

Modes of Operation

The AIM16-1/104 and AIM12-1/104 boards offer three software-selectable acquisition modes of operation. Interface to the host is by programmed I/O or DMA.

Mode 0

This mode of operation initiates a conversion each time any one of three preselected trigger signals occur. There are two programmable selections: a burst mode.and a non-burst mode. In the non-burst mode, only one conversion is made on one preprogrammed channel for each trigger. The conversion is synchronized to the trigger signal. In the burst mode, each preprogrammed channel will be converted once at a 100 kHz rate for each trigger signal.

Mode 1

This mode uses the external trigger or the software trigger to enable the 24-bit on-board trigger counter. The counter is loaded with a preset value and clocked until it overflows. Each time the counter overflows, a burst of conversions is initiated and each preprogrammed channel will be converted once at a 100 kHz rate. Conversions are synchronized to the on-board 10 MHz clock. The conversion process stops until the counter overflows again. This process continues until the software stops it by resetting the GO Bit.

Mode 2

This mode provides a means for taking continuous conversions through all preprogrammed channels at the maximum rate of the card. There are two programmable options to this mode. One uses the external trigger or the software trigger as a gate for taking conversions. The process continues until the external trigger or the software trigger is reset. The other option allows the internal trigger counter to set the GO Bit and start the conversion process. Conversions continue until the counter overflows stopping the process. All conversions in Mode 2 are synchronized to the onboard 10 MHz clock.

I/O Header

All I/O analog and digital signals are interfaced through a 40-pin right angle male header. The pinout is as follows.

AGND	1	2	Vref
Ch0	3	4	Ch 8 HI, 0 LO
Ch1	5	6	Ch 9 HI, 1 LO
Ch 2	7	8	Ch 10 HI, 2 LO
Ch 3	9	10	Ch 11 HI, 3 LO
Ch 4	11	12	Ch 12 HI, 4 LO
Ch 5	13	14	Ch 13 HI, 5 LO
Ch 6	15	16	Ch 14 HI, 6 LO
Ch 7	17	18	Ch 15 HI, 7 LO
AGND	19	20	+15V
−15V	21	22	DGND
D0	23	24	D1
D2	25	26	D3
D4	27	28	D5
D6	29	30	D7
D8	31	32	D9
D10	33	34	D11
D12	35	36	D13
D14	37	38	D15
Ext Trig	39	40	DGND

Software Description

"C" functions, with source code to control low level board interfacing, are provided with the AIM16-1/104 and AIM12-1/104 boards. Two sample routines (one acquisition under programmed I/O), the other under DMA are also provided.

WHAT IS PC/104?

The Need for an Embedded-PC Standard

Over the past decade, the PC architecture has become an accepted platform for far more than desktop applications. Dedicated and embedded applications for PCs are beginning to be found everywhere! PCs are used as controllers within vending machines, laboratory instruments, communications devices, and medical equipment, to name a few examples.

By standardizing hardware and software around the broadly supported PC architecture, embedded system designers can substantially reduce development costs, risks, and time. This means faster time to market and hitting critical market windows with timely product introductions. Another important advantage of using the PC architecture is that its widely available hardware and software are significantly more economical than traditional bus architectures such as STD, VME and Multibus. This means lower product costs.

For these reasons, companies that embed microcomputers as controllers within their products seek ways to reap the benefits of using the PC architecture. However, the standard PC bus form factor (12.4" x 4.8") and its associated card cages and backplanes are too bulky (and expensive) for most embedded control applications.

The only practical way to embed the PC architecture in space- and power-sensitive applications has been to design a PC — chip-by-chip — directly into the product.

But this runs counter to the growing trend away from "reinventing the wheel." Wherever possible, top management now encourages out-sourcing of components and technologies to reduce development costs and accelerate product design cycles.

A need therefore arose for a more compact implementation of the PC bus, satisfying the reduced space and power constraints of embedded control applications. Yet these goals had to be realized without sacrificing full hardware and software compatibility with the popular PC bus standard. This would allow the PC's hardware, software, development tools, and system design knowledge to be fully leveraged.

PC/104 was developed in response to this need. It offers full architecture, and hardware and software compatibility with the PC bus, but in ultra-compact (3.6" x 3.8") stackable modules. PC/104 is therefore ideally suited to the unique requirements of embedded control applications.

A Proposed Extension to IEEE-P996

Although PC/104 modules have been manufactured since 1987, a formal specification was not published until 1992. Since then, interest in PC/104 has skyrocketed, with numerous PC/104 modules introduced by more than one hundred manufacturers of PC/104-compatible products. Like the original PC bus, PC/104 is thus the expression of a de facto standard, rather than the invention and design of a committee.

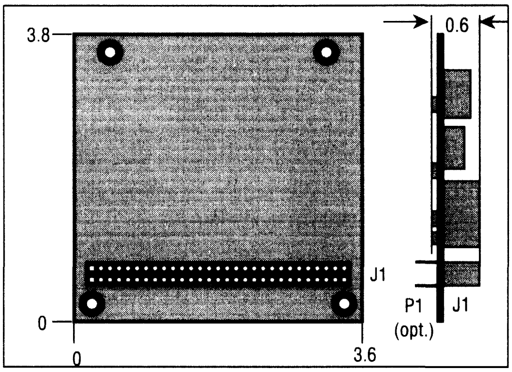


Figure 1. Basic Mechanical Dimensions (8-bit Version)

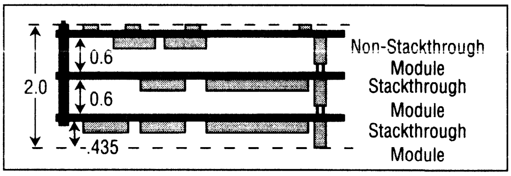


Figure 2. Standalone Board Stacks.

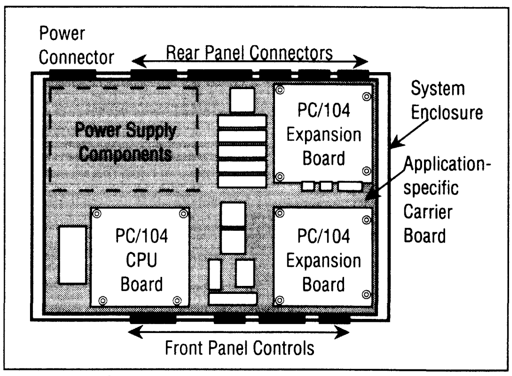


Figure 3. Component-like Applications

In 1992, the IEEE began a project to standardize a reduced form factor implementation of the IEEE P996 (draft) specification for the PC and PC/AT buses, for embedded applications. The PC/104 Specification has been adopted as the "base document" for this new IEEE draft standard, called the P996.1 Standard for Compact Embedded-PC Modules.

The key differences between PC/104 and the regular PC bus (IEEE P996) are:

- Compact form factor. Size reduces to 3.6 by 3.8 inches.
- Unique self-stacking bus. Eliminates the cost and bulk of backplanes and card cages.
- Pin-and-socket connectors. Rugged and reliable 64- and 40-contact male/female headers replace the standard PC's edgecard connectors.
- Relaxed bus drive (6 mA). Lowers power consumption (to 1-2 watts per module) and minimizes component count.

By virtue of PC/104, companies embedding PC technology in limited space applications can now benefit from a standardized system architecture complete with a wide range of multi-vendor support.

Two Ways to Use PC/104 Modules

Although configuration and application possibilities with PC/104 modules are practically limitless, there are two basic ways they tend to be used in embedded system designs:

Standalone Module Stacks: As shown in Figure 2, PC/104 modules are self-stacking. In this approach, the modules are used like ultra-compact bus boards, but without needing backplanes or card cages. Stacked modules are spaced 0.6 inches apart. (The three-module stack shown in Figure 2 measures just 3.6 by 3.8 by 2 inches.) Companies using PC/104 module stacks within their products frequently create one or more of their own application-specific PC/104 modules.

Component-Like Applications: Another way to use PC/104 modules is illustrated in Figure 3. In this configuration, the modules function as highly integrated components, plugged into custom carrier boards which contain application-specific interfaces and logic. The modules' self-stacking bus can be useful for installing multiple modules in one location. This facilitates future product upgrades or options, and allows temporary addition of modules during system debug or test.

About the PC/104 Consortium

The purpose of the PC/104 Consortium is to establish PC/104 as a broadly supported industry standard architecture for embedded-PC applications. The PC/104 Consortium maintains and distributes the PC/104 Specification and other PC/104-related documents, serves as a liaison to standards bodies such as IEEE P996.1, and engages in a variety of public relations activities on behalf of PC/104. Consortium membership is open to companies who offer or use PC/104 modules, as well as to companies who provide products that target PC/104 applications.

"What is PC/104?" reprinted courtesy of the PC/104 Consortium.

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Ordering Guide

Specify:

12-Bit, 16-Ch., Bipolar Analog Input Module	**AIM12-1/104B**
12-Bit, 16-Ch., Unipolar Analog Input Module	**AIM12-1/104U**
16-Bit, 16-Ch., Bipolar Analog Input Module	**AIM16-1/104B**
16-Bit, 16-Ch., Unipolar Analog Input Module	**AIM16-1/104U**
AIM16/12-1/104 User Manual	**16-400626**

(A manual is included free of charge with the placement of an initial order. To receive additional manuals, order 16-400626)

Signal Conditioning Modules

Selection Guide

SELECTION GUIDE

DCP5B Series, Analog I/O Signal Conditioning Modules

Model	Input Range	Bandwidth	Output Range	Page
DCP5B30-XX	±10 mV to±100 mV	4 Hz	±5V, 0V to +5V	163
DCP5B31-XX	±1V to ±10V	4 Hz	±5V, 0V to +5V	163
DCP5B40-XX	±10 mV to ±100 mV	10 kHz	±5V, 0V to +5V	163
DCP5B41-XX	±1V to ±10V	10 kHz	±5V, 0V to +5V	163
DCP5B39-XX	0V to +5V	4 Hz	0 or 4 to 20 mA	163
DCP5B32-XX	0 or 4 to 20 mA	4 Hz	0V to +5V	163

DCP5B Series, Sensor Input Modules

Model	Input Sensor	Output Range	Feature	Page
DCP5B34-XX	RTD	0 to +5V	2-, 3-, or 4-wire Input	163
DCP5B37-XX	Thermocouple	0 to +5V	with CJC	163
DCP5B45-XX	Pulse	0 to +5V	0 to 100 kHz	163
DCP5B47-XX	Thermocouple	0 to +5V	Linearized with CJC	163
DCP5B38-XX	Strain Gauge	±5V	Half and Full Bridge	163

DCP5BAF Series, Low Pass Active Filter Modules

Model	Input Frequency	Filter Type	Page
DCP5BAF-LPBU Series	1 kHz - 50 kHz	9-pole, Butterworth	173
DCP5BAF-LPBE Series	1 kHz - 50 kHz	9-pole, Bessel	173

D-Series, Sensor to Signal, Signal Conditioning Modules

Model	Transfer Function	Input	Output	Page
D-11XX	Fixed	Voltage	RS-232C/RS-485	177
D-12XX	Fixed	Current	RS-232C/RS-485	177
D-13XX	Fixed	Thermocouple	RS-232C/RS-485	177
D-14XX	Fixed	RTD	RS-232C/RS-485	177
D-15XX	Fixed	Bridge	RS-232C/RS-485	177
D-16XX	Fixed	Frequency & Pulse	RS-232C/RS-485	177
D-17XX	Digital I/O	Dig., RS-232C/RS-485	Dig., RS-232C/RS-485	177
D-21-XX	Programmable	Voltage	RS-232C/RS-485	177
D-22XX	Programmable	Current	RS-232C/RS-485	177
D-25XX	Programmable	Bridge	RS-232C/RS-485	177
D-26XX	Programmable	Frequency & Pulse	RS-232C/RS-485	177
D-31XX	Fixed	RS-232C/RS-485	Voltage	177
D-32XX	Fixed	RS-232C/RS-485	Current	177
D-41XX	Programmable	RS-232C/RS-485	Voltage	177
D-42XX	Programmable	RS-232C/RS-485	Current	177

Compact, Low Cost Modular Signal Conditioners

Designed for Laboratory and Industrial Applications

Introduction

The DCP5B Series represents an innovative generation of low cost, high performance plug-in signal conditioners. Designed for laboratory and industrial applications, these modules combine precision signal conditioning with transformer-based isolation. They are compact, economical components whose performance exceeds that available from more expensive non-isolated devices. Combining 1500V RMS continuous CMV isolation, ±0.05% calibrated accuracy, small size and low cost, the DCP5B Series provides an economical method of configuring a modular signal conditioning system.

All modules are hard-potted and identical in pin-out and size (2.28" x 2.26" x 0.60"). They can be mixed and matched, permitting users to address their exact needs, and may be changed without disturbing field wiring. The isolated input modules provide: 0 to +5V or ±5V outputs and accept J, K, T, E, R, S and B thermocouples; 100Ω platinum, 10Ω copper and 120Ω nickel RTDs; full or half bridge strain gages; mV, V, 4–20 mA or 0–20 mA, and wide bandwidth (10 kHz) mV and V signals. These modules feature complete signal conditioning functions including 240V RMS input protection, filtering, chopper-stabilized low drift (±1 μV/°C), amplification, 1500V RMS isolation, linearization for RTD and thermocouple (with DCP5B47) inputs and sensor excitation when required. The output modules convert ±5V or 0 to +5V inputs to isolated 4–20 mA or 0–20 mA process current signals. All modules feature excellent common mode rejection and meet ANSI/IEEE C37.90.1-1989 surge withstand specifications.

There is also a mounting backplane that provides a complete signal conditioning solution for end users. The DCPPB01 backplane incorporates screw terminals for field wiring inputs and outputs, as well as cold junction compensation sensors for thermocouple applications. Nineteen-inch relay rack-compatible units that can hold up to sixteen modules are also available.

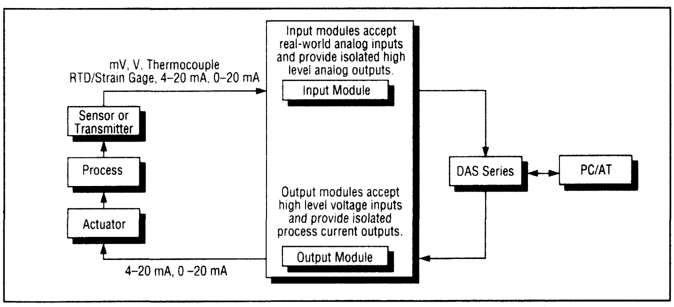
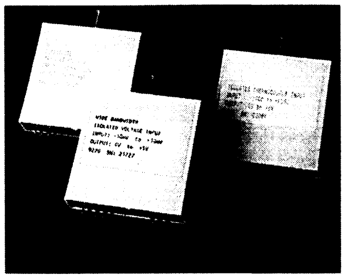


Figure 1. Functional Block Diagram of a measurement and control application using Analogic Data Acquisition Components.



Features

- ❑ Rugged, Compact, Low-Cost Signal Conditioners
- ❑ Analog Input Modules for Direct Interface to Sensors: Thermocouples, RTDs, and Strain Gages, Millivolt and Voltage Sources, 4–20 mA or 0–20 mA Process Current Inputs
- ❑ Analog Output Modules, 4–20 mA or 0–20 mA Process Current Output
- ❑ Complete Signal Conditioning function, 240V RMS Field Wiring Protection, Filtering, Amplification, 1500V RMS CMV Isolation, and High Noise Rejection
- ❑ High Accuracy: ±0.05%
- ❑ Low Drift: ±1 μV/°C
- ❑ –25°C to +85°C Temperature Range
- ❑ Mix and Match Module Capability
- ❑ Convenient Connection to User's Equipment
- ❑ Transient Protection–ANSI/IEEE C37.90.1-1989

DCP5B SERIES

Specifications[1]

MODEL	DCP5B30/5B31	DCP5B32	DCP5B34
Input Ranges[2]	DC mV/DC V	Process Current	RTD
Output Ranges	±5V 0 to +5V	0 to +5V	0 to +5V
Accuracy	±0.05% Span	•	See Ordering Guide
Nonlinearity	±0.02% Span	•	±0.05% Span Conformity
Stability			
Input Offset	±1 μV/°C/20 μV/°C	±50 nA/°C	±0.02°C/°C
Output Offset	±20 μV/°C	•	•
Span	±25 ppm/°C/±50 ppm/°C	±25 ppm/°C	±50 ppm/°C
Common Mode Voltage, Input to Output	1500V RMS continuous	•	•
Common Mode Rejection @ 50 Hz to 60 Hz	160 dB	•	•
Normal Mode Rejection @ 50 Hz or 60 Hz	95 dB/90 dB	•	•
Input Protection	240V RMS continuous	•	•
Output Resistance	50Ω	•	•
Voltage Output Protection	Continuous short to ground	•	•
Input Transient Protection	ANSI/IEEE C37.90.1-1989	•	•
Input Resistance	50 MΩ/650 kΩ	20.00Ω ±0.1%	50 MΩ
Bandwidth	4 Hz	•	•
Output Selection Time (to ±1μV of Vout)	3.5 μs (at 500 pF)	•	•
Power Supply	+5V DC ±5%	•	•
Size	2.28" x 2.26" x 0.6"	•	•
Environmental			
Operating Temperature Range	–25°C to +85°C	•	•
Storage Temperature Range	–40°C to +85°C	•	•
Relative Humidity	0 to 95% Noncondensing	•	•
RFI Susceptibility	±0.5% Span Error, 5W (@ 400 MHz @ 3 ft)	•	•

MODEL	DCP5B37/5B47	DCP5B40/5B41	DCP5B38
Input Ranges[2]	Thermocouple	Wideband dc mV/V	100/300Ω to 10 kΩ Bridges
Output Ranges	0 to +5V	0 to +5V, ±5V	±5V
Accuracy	±0.05%/ (see ordering guide)	±0.05% of Span	±0.08% of Span
Nonlinearity	±0.02% of Span/nA	•	•
Stability			
Input Offset	±1 μV/°C	±1 μV/°C/±20 μV/°C	±1 μV/°C
Output Offset	±20 μV/°C	±40 μV/°C	±40 μV/°C
Span	±25 ppm of rdg/°C	±25 ppm/°C/(±50)	±25 ppm of rdg/°C
Common Mode Voltage, Input to Output	1500V RMS continuous	•	•
Common Mode Rejection @ 50 Hz to 60 Hz			
1 kΩ Source Unbalance	160 dB	100 dB	100 dB
Normal Mode Rejection @ 50 Hz or 60 Hz	95 dB/90 dB	120 dB/decade	120 dB/decade
Differential Input Protection	240V RMS continuous	•	•
Output Resistance	50Ω	•	•
Voltage Output Protection	Continuous short to ground	•	•
Input Transient Protection	ANSI/IEEE C37.90.1-1989	•	•
Input Resistance	50 MΩ/650 kΩ	200 MΩ/650 kΩ	50 MΩ
Bandwidth (–3 dB)	4 Hz	10 kHz	•
Output Selection Time (to ±1mV of Vout)	3.5 μs (at 500 pF)	•	•
Power Supply	+5V ±5%	•	•
Size	2.28" x 2.26" x 0.6"	•	•
Environmental			
Operating Temperature Range	–25°C to +85°C	•	•
Storage Temperature Range	–40°C to +85°C	•	•
Relative Humidity / MIL Spec 202	0 to 95% Noncondensing	•	•
RFI Susceptibility	±0.5% Span Error, 5W (@ 400 MHz @ 3 ft)	•	•
Excitation Output V, 300Ω Load	–	–	+10V ±3 mV/+3.33V ±2 mV
Excitation Load Regulation	–	–	±5 ppm/mA
Excitation Stability	–	–	±15 ppm/°C
Half Bridge Voltage Level	–	–	Excitation V/2 ±1 mV

NOTES:

1. Typical @ +25°C and +5V Power.
2. See Ordering Guide for Input Ranges.

Specifications subject to change without notice.

DESIGN FEATURES AND USER BENEFITS

These signal conditioners are designed to provide an easy and convenient solution to signal conditioning problems of both designers and end users in measurement and control applications. Typical applications with DAS Series boards are standard data acquisition systems, programmable controllers, analog recorders, and dedicated control systems. The DCP5B Series modules are ideally suited to applications where monitoring and control of temperature, pressure, flow, and other analog signals are required.

System Solution

The DCP5B Series, in conjunction with any of the DAS Series PC/AT boards, provides a complete signal conditioning solution. Plug-in modules, factory precalibration of each unit, direct sensor interface via screw terminal connections, standardized high level outputs, and a cable system interface result in easy integration into any DAS-Series-based system. For thermocouple applications, high accuracy, cold junction compensation sensing is provided on each channel. A general subsystem application is outlined in Figure 1.

Flexibility

The DCP5B Series can be easily tailored to meet each user's needs. These plug-in signal conditioners can be mixed and matched to provide I/O for various process sensors and actuators.

High Reliability

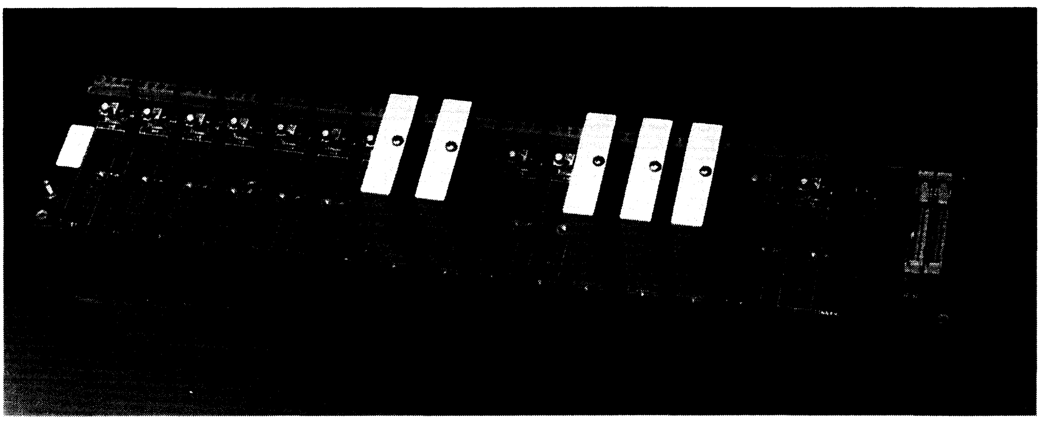
The DCP5B Series was designed to assure maximum reliability under real-world conditions. The modules are specified over the –25°C to +85°C temperature range. Each module is hard-potted; there are no adjustment potentiometers that could introduce mechanical and human errors that impair system integrity. All field-wired terminations, including sensor inputs, excitations and current outputs, are protected against continuous 240V RMS line voltage. This prevents a fault from damaging the module, the backplane, or other devices connected to the system. The modules also provide protection against high common mode voltages and are designed to meet the ANSI/IEEE standard for transient voltage protection.

High Performance

The high-quality signal conditioning features ±0.05% calibration accuracy, nonlinearity of only ±0.02% span and chopper-based amplification which ensures low drift (±1 μV/°C) and excellent long-term stability. Low drift sensor excitation is provided when required, and the RTD and thermocouple modules provide an output that is linear with temperature.

High Noise Rejection

The DCP5B Series modules were designed to accurately process low level signals in electrically noisy environments by providing 1500V RMS continuous transformer isolation, which eliminates ground loops, protects against transients, and solves common mode voltage problems. To further preserve signal integrity, 160 dB common mode rejection, 95 dB normal mode rejection, and excellent RFI/EMI immunity are provided.



DCP5B Series in 16 Position Mainframe.

DCP5B INPUT MODULES GENERAL DESCRIPTION

The galvanically-isolated DCP5B Series input modules are single-channel, plug-in signal conditioners that provide input protection, amplification and filtering, series output switching, and a high level analog output. Key specifications include: 1500V RMS isolation; accuracy of ±0.05%; ±0.02% span nonlinearity; and low drift of ±1 μV/°C. All modules operate from a single +5V supply with typical power consumption of 0.15W. The modules are hard-potted.

The transfer function provided by each input module is:

Input — specified sensor measurement range

Output — 0 to +5V or ±5V

Each DCP5B Series input module is available in a number of standard ranges.

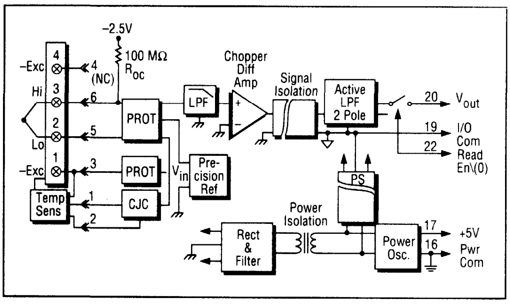


Figure 2. DCP5B37 Block Diagram.

DCP5B37 FUNCTIONAL DESCRIPTION

Figure 2 shows a functional diagram for a typical input module, the DCP5B37 thermocouple conditioner. The module provides cold junction compensation for the associated screw terminals as well as a bias current to give a predictable (upscale) response to an open thermocouple. Input protection allows safe operation, even in the event of a 240V RMS power line being connected to the signal terminals. In modules designed to work with sensors requiring excitation, low drift sensor excitation is provided and is protected at the same level.

A three-pole filter with a 4 Hz cutoff provides 95 dB of normal mode rejection and CMR enhancement at 60 Hz. One pole of this filter is located at the module input, while the other two poles are in the output stage for optimum noise performance. A chopper-stabilized input amplifier provides all of the module's gain for ultralow drift. This amplifier operates on the input signal after subtraction of a stable, laser-trimmed zero-suppression signal which sets the zero-scale input value. It is, therefore, possible to suppress a zero-scale input which is many times the total span to provide precise expanded scale measurements.

Signal isolation is provided by transformer coupling, using a modulation technique to provide exceptionally linear, stable performance at low cost. A demodulator on the output side of the signal transformer recovers the original signal, which is then filtered and buffered to provide a clean, low impedance output. A series output switch is included to eliminate the need for external multiplexing in many applications. This switch has a low output resistance (50Ω) and is controlled by an active-low enable input which is compatible with CMOS and LSTTL signals. In cases where the output switch is not used, such as single-channel and conventionally multiplexed applications, the enable input should be grounded to power common to turn on the switch.

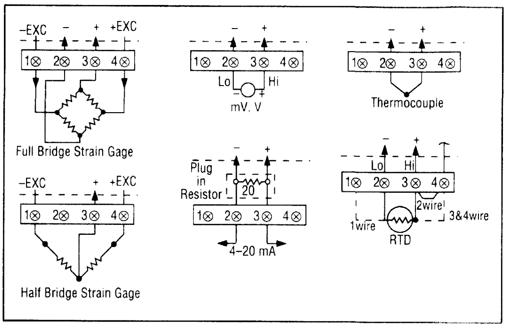


Figure 3. DCP5B Series Input Connections.

A single +5V power supply input (as used for all DCP5B Series modules) operates a clock oscillator which drives power transformers for the input and output circuits. The input circuit is, of course, fully floating. In addition, the output section acts as a third floating port, eliminating many problems that might be created by ground loops and supply noise. The common mode range of the output circuit is limited; however, output common must be kept within ±3V of power common, and a current path must exist between the two commons at some point for proper operation of the demodulator and output switch.

Isolated Millivolt and Voltage Input Models DCP5B30 and DCP5B31

Models DCP5B30 and DCP5B31 accept millivolt and voltage signals respectively and have a 4 Hz bandwidth.

Isolated Current Input Model DCP5B32

Model DCP5B32 accepts process current signals. A resistor is supplied to convert the signal current to a voltage, and, since that resistor cannot be protected against destruction in the event of inadvertent connection of the power, it is provided in the form of a separate pluggable resistor carrier assembly.

Isolated RTD Input Model DCP5B34

This RTD input module provides 3-wire lead resistance compensation and can be connected to 2-, 3- or 4-wire RTDs. The lead resistance effect is ±0.02°C/Ω for P+ and Ni RTDs, ±0.2°C/Ω for Cu. It provides a low drift sensor excitation current of 0.25 mA for the DCP5B34 or DCP5B34-N or 1.0 mA for the DCP5B34-C and produces an output signal that is linear with temperature achieving a conformity error of ±0.05% of span and accuracy, including conformity error, ranging from ±0.40°C to ±0.88°C.

Isolated Thermocouple Input Models DCP5B37 and DCP5B47

The isolated thermocouple models incorporate cold junction compensation circuitry, which provides an accuracy of ±0.05% of span. Open thermocouple detection (upscale) is also provided. Standard models are available for thermocouple types J, K, T, E, R, S and B. Model DCP5B47 provides a linearized 0–5V output signal for all thermocouple types.

Isolated Wideband Millivolt and Voltage Input Models DCP5B40 and DCP5B41

Models DCP5B40 and DCP5B41 accept millivolt and voltage signals respectively and have a 10 kHz bandwidth for interface to dynamic signals.

Isolated Wideband Strain Gage Input Model DCP5B38

The DCP5B38 accepts signals from full and half-bridge 100Ω to 10 kΩ, and 300Ω to 10 kΩ transducers. The DCP5B38 provides +3.333V or+10.0V excitation, a –5V to +5V output, and features a 10 kHz bandwidth.

DCP5B SERIES OUTPUT MODULE

General Description

The DCP5B39 Current Output Module accepts a high level analog signal at its input and provides a 4–20 mA or 0–20 mA process current signal at its output. The module features high accuracy of ±0.05% and 1500V RMS common mode voltage isolation protections.

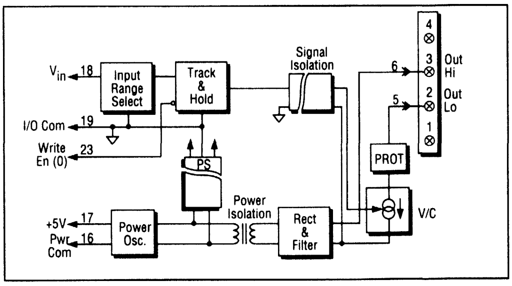


Figure 4. DCP5B39 Block Diagram.

The transfer function provided by this module is:

Input — 0 to –5V or ±5V

Output— 4–20 mA or 0–20 mA

To provide this range of functions, four varieties of the DCP5B39 are available; unipolar or bipolar input and 4-20 mA or 0-20 mA output. Range must be specified when ordering.

DCP5B39 Functional Description

Figure 4 is a functional block diagram of the DCP5B39 current output module. The voltage input, usually from a digital-to-analog converter, is buffered, and a quarter scale offset is added if a 4–20 mA output is specified.

The signal is latched in a track-and-hold circuit. This track-and-hold allows one DAC to serve numerous output channels. The output droop rate is 40 μA/s, which corresponds to a refresh interval for 0.01% FS droop of 50 ms. The track-and-hold is controlled by an active-low enable input, which is compatible with CMOS and LSTTL signals. In conventional applications where one DAC is used per channel and the track-and-hold is not used, the enable input should be grounded to power common. This keeps the module in tracking mode.

The signal is sent through an isolation barrier to the current output (V-to-I converter) stage. Signal isolation is proved by transformer coupling using a proprietary modulation technique for linear, stable performance at low cost. A demodulator on the output side of the signal transformer recovers the original signal, which is then filtered and converted to a current output. Output protection allows safe operation even in the event of a 240V RMS power line being connected to the signal terminals.

A single +5V supply powers a clock oscillator which drives power transformers for the input circuit and the output's high compliance, current loop supply. The output current loop is fully floating. In addition, the input section acts as a third floating port, eliminating many problems that might be created by ground loops and supply noise. The common mode range of the input circuit is limited; however, input common must be kept with ±1V of power common, and a current path must exist between the two commons at some point for proper operation of the track-and-hold control input.

OUTPUT MODULE SPECIFICATIONS

(Typical @ +25°C and +5V power)	
Input Ranges	0 to +5V or ±5V
Output Ranges	4–20 mA or 0–20 mA
Load Resistance Range[1]	0 to 650Ω
Accuracy[2]	±0.05% Span
Nonlinearity	±0.02% Span
Stability vs. Ambient Temperature	
Zero	±0.5 µA/°C
Span	±20 ppm of Span/°C
Common Mode Voltage, Output to Input and Power Supply	1500V RMS continuous
Common Mode Rejection	110 dB
Normal Mode Output Protection	240V RMS continuous
Output Transient Protection	Meets ANSI/IEEE C37.90.1-1989
Sample-and-Hold	
Output Droop Rate	40 µA/s
Acquisition Time	50 µs
Overrange Capability	10%
Maximum Output Under Fault	26 mA
Input Resistance	50 MΩ
Bandwidth (–3 dB)	400 Hz
Power Supply	+5 VDC ±5%
Maximum Input Voltage Without Damage	±36V
Size	2.28" x 2.26" x 0.6"
Environmental	
Operating Temperature Range	–25°C to +85°C
Storage Temperature Range	–40°C to +85°C
Relative Humidity Conforms to MIL Spec 202	0 to 95% noncondensing
RFI Susceptibility	±0.5% span error, 5W (@ 400 MHz @ 3 ft)

NOTES

1. With a minimum power supply voltage of 4.95V, R_1 can be up to 750Ω.
2. Accuracy specification includes the combined effects of repeatability, hysteresis and linearity. Does not include signal source error.

DCP5B SERIES SYSTEM CONFIGURATION

Design Application Information

The DCP5B Series was designed to facilitate integration by a system designer into a circuit board or backplane. Only a single 3.0 mm threaded insert is required to secure the module to a PC board. Module pins are accommodated by widely available sockets, and temperature sensors for thermocouple cold junction compensation are available as one-piece precalibrated units.

The DCP5B Series was also designed to minimize system interface space and cost. Each input module has an internal series output switch controlled by a TTL-compatible enable input, eliminating the need for external multiplexers so all modules can be served by a single input bus. Each output module has a track-and-hold input which allows a single digital-to-analog converter to serve numerous channels. Alternatively, the module enable lines can be grounded, the DCP5B Series input modules can be used with a conventional external MUX, and the output modules with a DAC per channel.

Ease of system application of these modules is enhanced by the fact that the output modules have enable and signal input pin assignments which do not coincide with the enable and signal output pins of the input modules (see Figure 7). This means that, in a single mix-and-match backplane environment, the reading of inputs and the writing and refreshing of outputs are completely independent and can occur simultaneously. For example, the input system may dwell for a long time on a single channel to collect thousands of samples without having to interrupt the process to do an output refresh or set a new output value. Similarly, a "dumb" refresh circuit can be built that can maintain outputs without even knowing which channels have

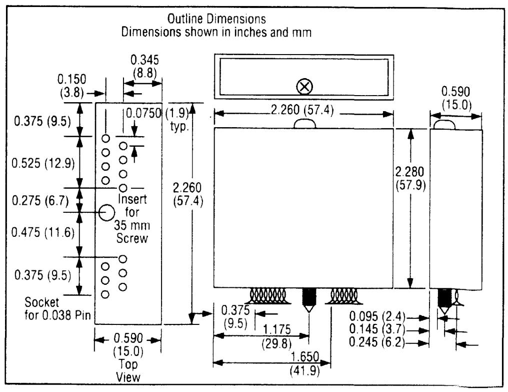


Figure 5. Module Footprint and Pinout.

output modules; it can refresh all channels, and those that are inputs will ignore the operation.

Backplane Functional Description

The DCP5B Series includes a mounting backplane. A 16-channel backplane can be mounted in a 19" x 3.5" panel space. Each channel has four screw terminals for field connections. The connections satisfy all transducer inputs and process current outputs, and provide transducer excitation when necessary. A cold junction sensor is supplied on each channel to accommodate thermocouple modules. A system interface B01 provides high level voltage I/O for all channels. The DCP5B Series backplane requires a +5V external power source (DCPXPRT/E-003).

The DCPPB01, diagrammed in Figure 6, provides sixteen single-ended input/output pins on the system connector.

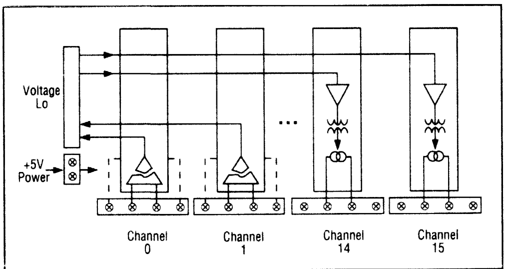


Figure 6. DCPPB01 Block Diagram.

Backplane Specifications	
	DCPPB01
Channels	16
External Power Requirement	+5V
Cold Junction Sensor	On Each Channel
Physical Size	3.5" x 17.4" (88.9 mm x 442 mm)

Interface Pin Designations

WRITE EN (0) 23	22 READ EN (0)
RESERVED 21	20 V_{out}
I/O COM 19	18 V_{in}
+5V 17	16 POWER COM
IN LO 5	6 IN HI
–EXC 3	4 +ESC
SENSOR– 1	2 SENSOR +

DCPPB01

CH 0 1	o	o	2 CH 8
COM 3	o	o	4 CH 9
CH 1 5	o	o	6 COM
CH 2 7	o	o	8 CH 10
COM 9	o	o	10 CH 11
CH 3 11	o	o	12 COM
CH 4 13	o	o	14 CH 12
COM 15	o	o	16 CH 13
CH 5 17	o	o	18 COM
CH 6 19	o	o	20 CH 14
COM 21	o	o	22 CH 15
CH 7 23	o	o	24 COM
SENSE 25	o	o	26 NC

Figure 7. System Connector Pin-out.

Ordering Guide

DCP5B Series Voltage Input Modules

Model	Input Range	Bandwidth	Output Range	Part Number
DCP5B30	±10 mV	4 Hz	±5V	DCP5B30-01
	±50 mV	4 Hz	±5V	DCP5B30-02
	±100 mV	4 Hz	±5V	DCP5B30-03
	±10 mV	4 Hz	0 to +5V	DCP5B30-04
	±50 mV	4 Hz	0 to +5V	DCP5B30-05
	±100 mV	4 Hz	0 to +5V	DCP5B30-06
DCP5B31	±1V	4 Hz	±5V	DCP5B31-
	±5V	4 Hz	±5V	DCP5B31-02
	±10V	4 Hz	±5V	DCP5B31-03
	±1V	4 Hz	0 to +5V	DCP5B31-04
	±5V	4 Hz	0 to +5V	DCP5B31-05
	±10V	4 Hz	0 to +5V	DCP5B31-06
DCP5B40	±10 mV	10 kHz	±5V	DCP5B40-01
	±50 mV	10 kHz	±5V	DCP5B40-02
	±100 mV	10 kHz	±5V	DCP5B40-03
	±10 mV	10 kHz	0 to +5V	DCP5B40-04
	±50 mV	10 kHz	0 to +5V	DCP5B40-05
	±100 mV	10 kHz	0 to +5V	DCP5B40-06
DCP5B41	±1V	10 kHz	±5V	DCP5B41-01
	±5V	10 kHz	±5V	DCP5B41-02
	±10V	10 kHz	±5V	DCP5B41-03
	±1V	10 kHz	0 to +5V	DCP5B41-04
	±5V	10 kHz	0 to +5V	DCP5B41-05
	±10V	10 kHz	0 to +5V	DCP5B41-06

DCP5B Series Current Input Modules

	Input Range	Bandwidth	Output Range	Part Number
DCP5B32	4 to 20 mA	4 Hz	0 to +5V	DCP5B32-01
	0 to 20 mA	4 Hz	0 to +5V	DCP5B32-02

DCP5B Series Isolated Input Modules — 2, 3 or 4 wire RTD Input

	Sensor	Range	Output	Accuracy*	Part Number
DCP5B34	100Ω platinum	–100° to 100°C	0 to +5V	±0.46°C	DCP5B34-P01
	100Ω platinum	0° to 100°C	0 to +5V	±0.36°C	DCP5B34-P02
	100Ω platinum	0° to 200°C	0 to +5V	±0.46°C	DCP5B34-P03
	100Ω platinum	0° to 600°C	0 to +5V	±0.88°C	DCP5B34-P04
	10Ω copper (at 0°C)	0° to 120°C	0 to +5V	±0.77°C	DCP5B34-C01
	10Ω copper (at 25°C)	0° to 120°C	0 to +5V	±0.77°C	DCP5B34-C02
** Includes Conformity*	120Ω nickel	0° to 300°C	0 to +5V	±0.40°C	DCP5B34-N01

DCP5B Series Thermocouple Input Modules with Cold Junction Compensation

	Thermocouple Type	Temperature Range	Output	Part Number
DCP5B37	J	–100° to 760°C	0 to +5V	DCP5B37-J01
	K	–100° to 1350°C	0 to +5V	DCP5B37-K02
	T	–100° to 400°C	0 to +5V	DCP5B37-T03
	E	0° to 900°C	0 to +5V	DCP5B37-E04
	R	0° to 1750°C	0 to +5V	DCP5B37-R05
	S	0° to 1750°C	0 to +5V	DCP5B37-S05
	B	0° to 1800°C	0 to +5V	DCP5B37-B05

DCP5B Series Current Output Modules

	Input Range	Output Range	Part Number
DCP5B39	0 to +5V	4 to 20 mA	DCP5B39-01
	–5V to +5V	4 to 20 mA	DCP5B39-02
	0 to +5V	0 to 20 mA	DCP5B39-03
	–5V to +5V	0 to 20 mA	DCP5B39-04

Ordering Guide (continued)

Frequency Input Modules

DCP5B45	Input Range	Output Range	Part Number
	0 to 500 Hz	0V to 5V	DCP5B45-01
	0 to 1 kHz	0V to 5V	DCP5B45-02
	0 to 3 kHz	0V to 5V	DCP5B45-03
	0 to 5 kHz	0V to 5V	DCP5B45-04
	0 to 10 kHz	0V to 5V	DCP5B45-05
	0 to 25 kHz	0V to 5V	DCP5B45-06
	0 to 50 kHz	0V to 5V	DCP5B45-07
	0 to 100 kHz	0V to 5V	DCP5B45-08

DCP5B Series Linearized Thermocouples

DCP5B47	Thermocouple Type	Temperature Range	Output	Accuracy	Part Number
	J	0° to 760°C	0 to 5V	±0.76°C	DCP5B47-J01
	J	–100° to 300°C	0 to 5V	±0.40°C	DCP5B47-J02
	J	0° to 500°C	0 to 5V	±0.36°C	DCP5B47-J03
	K	0° to 1000°C	0 to 5V	±1.0°C	DCP5B47-K04
	K	0° to 500°C	0 to 5V	±0.38°C	DCP5B47-K05
	T	–100° to 400°C	0 to 5V	±1.1°C	DCP5B47-T06
	T	0° to 200°C	0 to 5V	±0.30°C	DCP5B47-T07
	E	0° to 1000°C	0 to 5V	±1.5°C	DCP5B47-E08
	R	500° to 1750°C	0 to 5V	±1.6°C	DCP5B47-R09
	S	500°C to 1750°C	0 to 5V	±1.5°C	DCP5B47-S10
	B	500° to 1800°C	0 to 5V	±3.3°C	DCP5B47-B11

DCP5B Series Strain Gage Input Modules

DCP5B38	Input	Sensitivity	Excitation	Transducer Impedance	Output Range	Part Number
	Half Bridge	3 mV/V	3.333V	100Ω to 10 kΩ	±5V	DCP5B38-03
	Half Bridge	3 mV/V	10V	300Ω to 10 kΩ	±5V	DCP5B38-04
	Full Bridge	2 mV/V	10V	300Ω to 10 kΩ	±5V	DCP5B38-05

Accessories

Description	Part Number
DCP5B Interface Box (DCP5B-to-DAS)	STB-5B
19" Rack Mount, 16 Position Backplane	DCPPB01
Metal Rack and Mounting Kit for DCPPB01	DCPXRK-002
Single Channel DCP5B Mounting Panel	DCPPB03
Two Channel DCP5B Mounting Panel	DCPPB04
+5V @ 3A Power Supply – 120 VAC – U.S.	DCPXPRT-003
+5V @ 3A Power Supply – 220 VAC – European	DCPXPRE-003
Analog Interface Cable to DAS	ACAB-22/LN

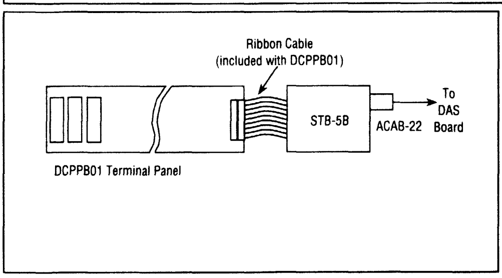


Figure 8. Typical DCP5B-to-DAS Board Configuration.

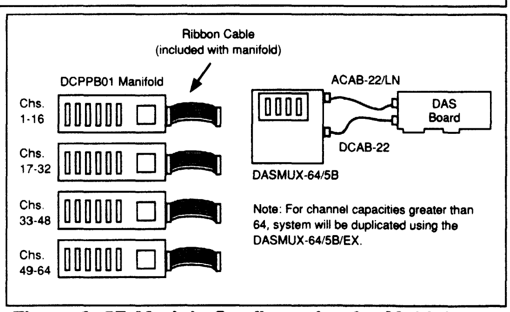


Figure 9. 5B Module Configuration for Multiple Manifolds.

Low-Pass Active Filter Modules

9-pole Linear Active Filters

Introduction

The DCP5BAF Series modules are 9-pole linear active filters, pinout- and package-compatible with the Analogic DCP5B Series of signal conditioning modules. They may be used together with, or independently from, the DCP5B signal conditioners.

The DCP5BAF filters are available in both Butterworth and Bessel configurations with 54 dB per octave roll-offs. The Series is ideally suited for use as anti-aliasing, noise reduction, or reconstruction filters. The ±10 volt input range with an overall gain of 1 makes the filters an excellent match to both the transducer output (from the signal source) and the data acquisition board input.

An internal DC/DC converter allows the modules to be operated from a non-critical +5 ±10% volt power source. This can be a key factor in many systems since logic power (+5V) is readily available in most systems while analog power (±12 or 15V) is much less common.

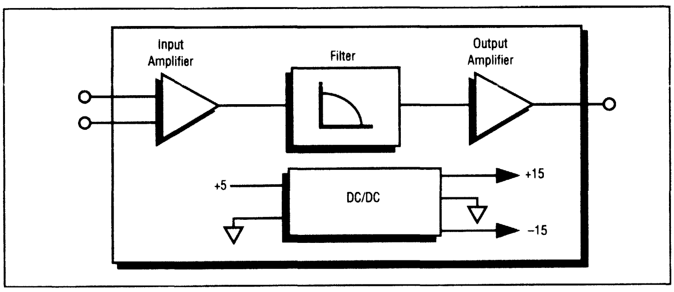
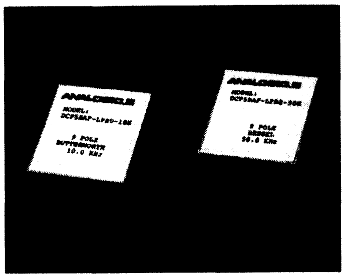


Figure 1. DCP5BAF Series Block Diagram.



Features

- ❑ Compatible with DCP5B Series Module
- ❑ 9-Pole (54 dB per Octave) Roll-offs
- ❑ Fully Differential Inputs
- ❑ 1, 2, 5, 10, 20 and 50 kHz Corner Frequencies

Applications

- ❑ Anti-aliasing Filters
- ❑ Industrial and Process Control
- ❑ Noise Reduction
- ❑ Reconstructive Filtering
- ❑ Test Systems

DCP5BAF SERIES

Specifications

ANALOG INPUT

Input Range
±10V

Differential Gain
1.0±0.03%

Input Impedance
20 kΩ ±10%

Common Mode Range
±20V

Common Mode Rejection
74 dB Min. at 1 kHz

Maximum Safe Input Voltage
±40V

ANALOG OUTPUTS

Offset Voltage
±3 mV

Offset Drift
±100 μV/°C

2Gain Drift
±30 ppm/°C

Noise (DC-50 kHz)
75 μV RMS Max.

Linear Operating Range
±10V at 2 mA

Output Impedance
1Ω Typ., 10Ω Max.

Max. Output Load
Short circuit protected

FILTER CHARACTERISTICS

Response Type
9-pole low-pass, Butterworth or Bessel characteristics

Cut-off Frequency Tolerance
±2%

Corner Frequencies
1.00 kHz, 2.00 kHz, 5.00 kHz, 10.0 kHz, 20.0 kHz and 50.0 kHz

POWER CONSUMPTION

+5V Supply
110 mA Typ., 125 mA Max. (1–20 kHz); 120 mA Typ., 135 mA Max. (50 kHz)

ENVIRONMENTAL

Operating Temperature
0 to +50°C

Storage Temperature
–20°C to +70°C

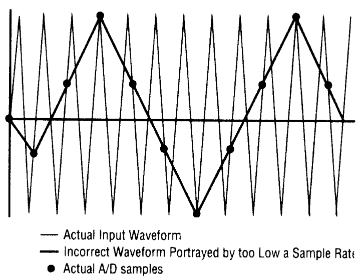
Humidity
0 to 95% non-condensing

Altitude
10,000 feet Max.

Specifications subject to change without notice.

Aliasing

When sampling an analog input, the data acquisition system can incorrectly show a slow moving signal that, in actuality, is at a higher frequency. This aliasing effect is shown in the diagram below. It can be caused by either incorrect sampling speed of the data acquisition system itself or by imposed noise overlaying the desired signal to be sampled. In the case of incorrect sampling, the Nyquist criterion imposes a limit of 0.5 times the sampling rate of the data acquisition system on input signal bandwidth. Adhering to this specification ensures accurate signal sampling.



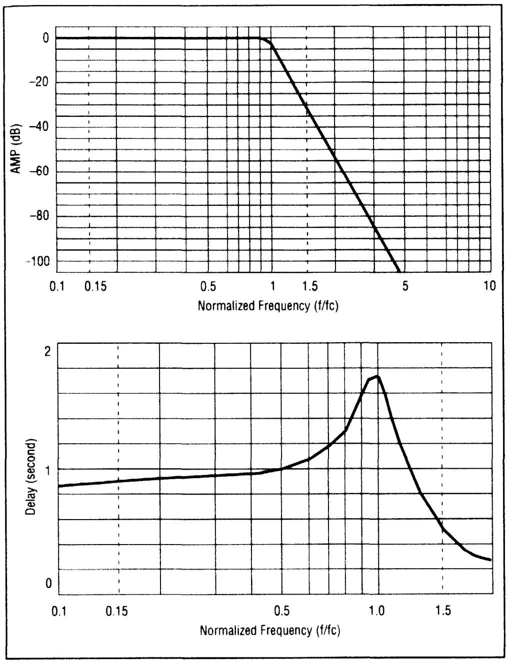
In the case of imposed random noise at a frequency greater than the system's sample rate, as is often encountered in less-than-ideal data acquisition conditions, erroneous sampling of the noise as well as the desired signal may occur.

An anti-aliasing filter is simply a low-pass filter with very sharp corner frequency roll-off that allows the true signal to pass while removing the undesired higher frequency noise component. Typically, the anti-aliasing filter cutoff frequency is set to 0.5 times the sample rate to assure the integrity of the measured signal.

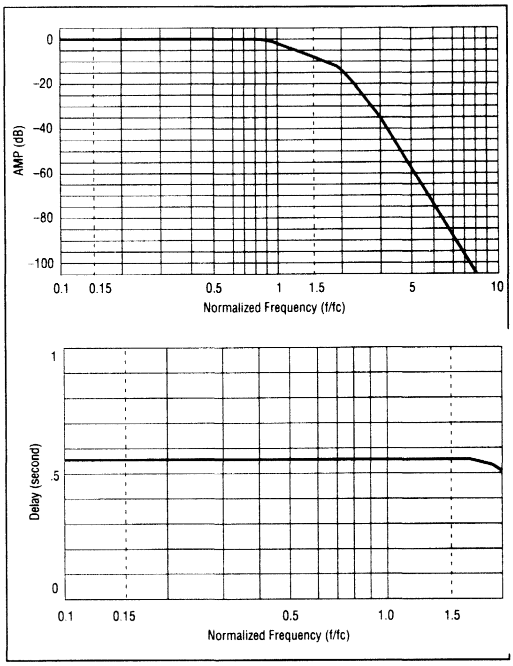
Top View

23	22
21	20 V_{OUT}
I/O COM 19	18
+5V 17	16 POWER COM
IN LO 5	6 IN HI
3	4
1	2

Connector Pin Assignment.



Butterworth



Bessel

Butterworth Versus Bessel

Depending on the application, either Butterworth or Bessel filter characteristics will provide the best performance. Butterworth filters offer the flat passband responses and sharp cut-offs required in anti-aliasing and noise-reduction systems. For these reasons, Butterworth filters are the most commonly used filter; however, they also induce significant distortion in the form of phase delay. In closed-loop systems and signal reconstruction applications, phase distortion can often be more important than pure roll-off rate. In these applications the Bessel filter is a better choice. The amplitude and phase performance of 9-pole Butterworth and Bessel filters are shown in the diagrams above.

Ordering Guide

Butterworth	
DCP5BAF-LPBU-1.0K	1.00 kHz 9-pole Butterworth Filter
DCP5BAF-LPBU-2.0K	2.00 kHz 9-pole Butterworth Filter
DCP5BAF-LPBU-5.0K	5.00 kHz 9-pole Butterworth Filter
DCP5BAF-LPBU-10.0K	10.0 kHz 9-pole Butterworth Filter
DCP5BAF-LPBU-20.0K	20.0 kHz 9-pole Butterworth Filter
DCP5BAF-LPBU-50.0K	50.0 kHz 9-pole Butterworth Filter
Bessel	
DCP5BAF-LPBE-1.0K	1.00 kHz 9-pole Bessel Filter
DCP5BAF-LPBE-2.0K	2.00 kHz 9-pole Bessel Filter
DCP5BAF-LPBE-5.0K	5.00 kHz 9-pole Bessel Filter
DCP5BAF-LPBE-10.0K	10.0 kHz 9-pole Bessel Filter
DCP5BAF-LPBE-20.0K	20.0 kHz 9-pole Bessel Filter
DCP5BAF-LPBE-50.0K	50.0 kHz 9-pole Bessel Filter
Accessories	
STB-5B	DAS-to-DCP5B Interface
DCPXPRT-003	Power Supply, 120 Vac Input
DCPXPRE-003	Power Supply, 220 Vac Input
DCPPB01	16-Position Mounting Rack

D-1000/D-2000/D-3000/D-4000

RS-232/RS-485-Compatible & Programmable Signal Conditioning Modules

Introduction

The D-1000 Series family of signal conditioning modules consists of the D-1000/2000 input modules and the D-3000/4000 output modules. These modules are designed to be mounted remotely from a host computer and communicate through standard RS-232 or RS-485 serial ports. All modules in the family use simple ASCII command/response-type protocol. Multi-drop capability allows up to 124 modules to share a single serial bus. In addition, all members of the family are fully compatible with each other. This allows unlimited mixing of input and output modules to meet the application need.

The D-1000 Series modules accept real-world input signals, perform the A/D conversions, convert the data into engineering units, and transmit this data to the host computer over an RS-232 or RS-485 serial interface. Most analog input modules also provide two digital output bits suitable for controlling solid-state relays or similar devices. Alarm limits (stored in non-volatile RAM so that data is not lost during power loss) can be set to control the digital outputs, or the outputs can be controlled by the serial interface port. All module configuration data such as module address (for multi-drop applications), baud rate, etc., are also stored in the non-volatile RAM.

Input modules measure temperature (with thermocouple or RTDs), voltage, current, frequency, events (pulse), bridge circuits (e.g., load cells, strain gauges) and digital I/O. The modules can be mixed and matched in any manner on a bus and can be placed up to 4000 feet from the host computer.

The D-1000 Series command set provides a simple and quick way to read data, read alarms, control digital I/O, etc. All modules contain screw terminal connections to simplify field wiring. The small size and form factor allow the modules to be mounted in virtually any location with a minimum of effort and required wiring.

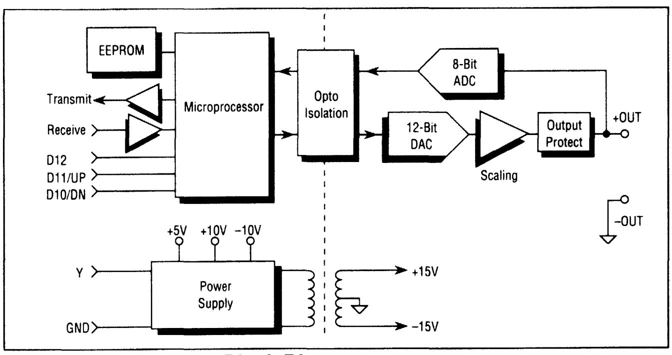
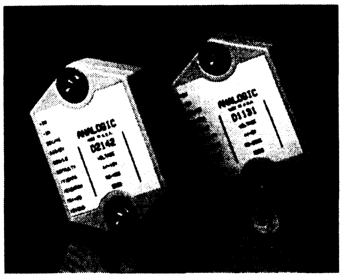


Figure 1. D-3000/4000 Block Diagram.



Features

- ❑ Complete Sensor-to-Serial Interface (D-1000/2000)
- ❑ Complete Computer-to-Analog Out Interface (D-3000/4000)
- ❑ 15-Bit Resolution (Input Modules)
- ❑ 12-Bit Resolution (Output Modules)
- ❑ Simple ASCII Command/Response Protocol
- ❑ Up to 124 Addressable Modules per Serial Port
- ❑ Operates on Single Unregulated Supply (10–30 VDC)
- ❑ All D-1000 Series Modules Fully Compatible with Others

Applications

- ❑ Remote Sensing/Control
- ❑ Environmental Measurements
- ❑ Datalogging
- ❑ Direct Connect to Modems

D-1000/D-2000

ANALOG
Single channel analog input
Maximum CMV, 500V RMS input to output @ 60 Hz
15-bit measurement resolution
Leakage current, input to output @ 115V RMS, 60 Hz <2 μA RMS
8 conversions per second
Autozero
Autocalibration
No adjustment pots

DIGITAL
8-bit CMOS microcomputer
All scaling, linearization and calibration performed digitally
Nonvolatile memory eliminates pots and switches

DIGITAL FILTERING
Small and large signal with user-selectable time constants from 0 to 16 seconds

DIGITAL INPUTS
Voltage Levels
+30V without damage
Switching Levels
High, 3.5V min., Low, 1.0V max.
Internal pull up resistors for direct switch input
(Excluding D-1711/1712 modules)

DIGITAL OUTPUTS
Open collector to 30V, 30 mA max. load

ALARM OUTPUTS
HI/LO limit checking by comparing input values to downloaded HI/LO limit values stored in memory

ALARMS
Latching (stays on if input returns to within limits) or momentary (turns off if inputs return to within limits)

COMMUNICATIONS
RS-232C, RS-485
Up to 124 multidrop modules per host communication port
User-selectable channel address
Selectable Baud Rates
300, 600, 1200, 2400, 4800, 9600, 19200, 38400
ASCII format command response protocol
Can be used with "dumb" terminal
Parity options: odd; even; none
All communications setups (address, baud rate, parity) stored in nonvolatile memory
Checksum can be added to any command or response
Communications distance up to 10,000 feet

EVENT COUNTER
Up to 10 million positive transitions @ 60 Hz max. filtered for switch debounce

POWER REQUIREMENTS
+10 to +30 VDC, 0.75W, typ.
(D1500/2500 = 2.0W max.)

ENVIRONMENTAL
Temperature Range
Operating –25°C to +70°C
Storage
–25°C to +85°C
Relative Humidity
0 to 95% non-condensing

D-3000/D-4000

ANALOG OUTPUT
Single-channel analog output
Voltage
0–1V, ±1V, 0–5V, ±5V, 0–10V, ±10V
Current
0–20 mA, 4–20 mA
Input isolation to 500V RMS
12-bit measurement resolution

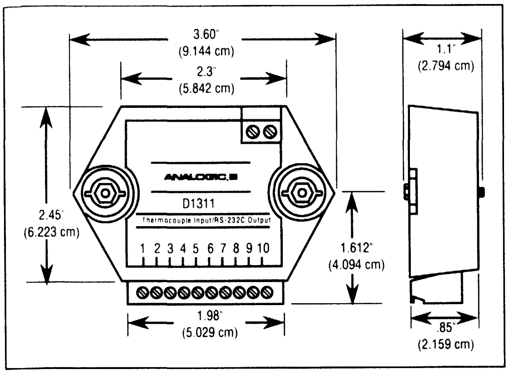
ACCURACY (INTG. & DIFF. NONLIN.)
0.1% FS (max.) accuracy over temperature
1000 conversions per second
Settling Time to 0.1% FS 300 μs typ. (1 ms max.)
Output Slewing Manual Mode (–FS to +FS): 5s
Programmable Output Slew Rate: 0.1V/s (mA/s) to 10,000V/s (mA/s) (D-4000)
Autozero & Autocalibration
No adjustment pots
Voltage Compliance
+12V
Output Drive, Short Circuit Current
5 mA min., 10 mA max.

ANALOG OUTPUT READBACK (D-4000)
8-bit analog-to-digital converter
Accuracy over temperature
–25°C to +70°C; 2.0% FS max.

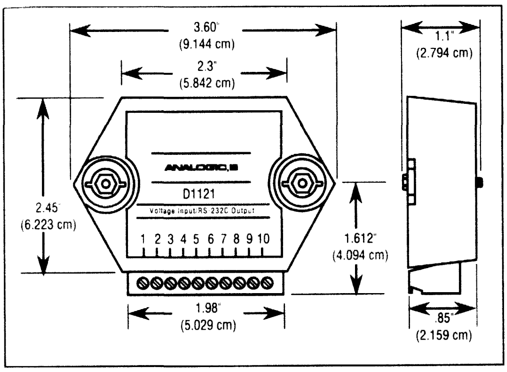
DIGITAL
8-bit CMOS microcomputer
Digital scaling and calibration
Nonvolatile memory eliminates pots and switches
Programmable data scaling (D-4000)
Programmable High/Low output limits
Programmable initial value (D-4000)
Programmable watchdog timer provides orderly shut-down in the event of host failure (D-4000)

MECHANICALS AND DIMENSIONS
Case
ABS w/captive mounting hardware
Connectors
Screw terminal barrier plug (supplied)
Replace with Phoenix MSTB 1.5/10 ST 5.08 or equivalent
Note:
Spacing for mounting screws = 2.700" (6.858 cm). Screw threads are 6 x 32.

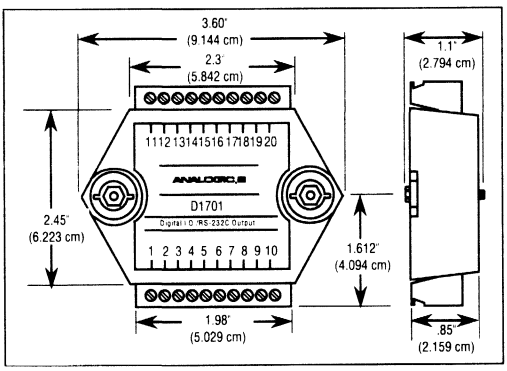
Specifications subject to change without notice.



D-1300 Series.



D-1000/D-2000 Series.



D-1700 Series.

The D-2000 Series modules are programmable versions of the D-1000 modules. Unlike the D-1000 with its fixed transfer function, the D-2000 modules are designed to allow the user to create custom non-linear transfer functions. This feature is used to linearize non-standard sensors and provide outputs scaled in engineering units. The D-2000 modules can be programmed to approximate square, root, log, high-order polynomial, or any other nonlinear function. The D-2000 Series can also be empirically field programmed when the exact transfer function is unknown.

The D-2000 modules typically contain two digital outputs and one digital input. The digital outputs consist of open collector transistor switches that are controlled by the host computer. These switches are used to control solid-state relays for heater control, pump and other power equipment control. The digital input can be read by the host and used to sense the condition of a remote digital signal.

Digital high and low alarm functions are included in all D-2000 modules. High and low limit data can be downloaded to the module by the host computer. The limit data is compared against the analog input data after every A/D conversion. The results of the limit comparison can be read by the host. The high and low limits can also be used to control the digital output lines on the module.

The D-3000 Series modules are complete computer-to-analog output devices. They are mounted remotely from the host computer and communicate with standard RS-232 or RS-485 serial ports. Simple ASCII commands are used to control a 12-bit digital-to-analog converter (DAC) that is scaled to provide commonly used voltage and current ranges. An on-board microprocessor is used to provide the communications interface and many intelligent analog output functions.

the D-4000 Series modules are similar in form and function to the D-3000 modules. However, the D-4000 modules are designed to offer many intelligent features. These features include fully programmable output slew rates, programmable data scaling, true analog read back of the output signal, programmable initial values and a watchdog timer that provides orderly shutdown in the event of host failure.

The A-1000 converter boxes provide a simple way to convert RS-232 communications standards to the correct electrical signals required by RS-485. The D-1000 box converts RS-232 to RS-485. The D-1300 box is a RS-485 repeater. The RS-485 standard is the preferred method for field communication when many D-Series modules are interfaced to a host computer over long distances. The converter boxes permit data transmission up to 4000 feet at baud rates up to 115.5K. The converter boxes also automatically control the bus direction without handshaking signals for the host. In addition, each converter box provides power (+24V @ 1 amp) that can drive D-Series modules.

D-1000 Series: Model	Input/Output
	Voltage Inputs
D-1111	100 mV Input/RS-232C Output
D-1112	100 mV Input/RS-485 Output
D-1121	1V Input/RS-232C Output
D-1122	1V Input/RS-485 Output
D-1131	5V Input/RS-232C Output
D-1132	5V Input/RS-485 Output
D-1141	10V Input/RS-232C Output
D-1142	10V Input/RS-485 Output
D-1151	100V Input/RS-232C Output
D-1152	100V Input/RS-485 Output
	Current Inputs
D-1221	1 mA Input/RS-232C Output
D-1211	10 mA Input/RS-232C Output
D-1231	100 mA Input/RS-232C Output
D-1232	100 mA Input/RS-485 Output
D-1251	4–20 mA Input/RS-232C Output
D-1252	4–20 mA Input/RS-485 Output
	Thermocouple Inputs
D-1311	J-Type Input/RS-232C Output
D-1312	J-Type Input/RS-485 Output
D-1321	K-Type Input/RS-232C Output
D-1322	K-Type Input/RS-485 Output
D-1331	T-Type Input/RS-232C Output
D-1332	T-Type Input/RS-485 Output
D-1361	S-Type Input/RS-232C Output
D-1362	S-Type Input/RS-485 Output
	RTD Inputs
D-1411	0.00385 RTD In/RS-232C Output
D-1412	0.00385 RTD In/RS-485 Output
D-1421	0.00392 RTD In/RS-232C Output
D-1422	0.00392 RTD In/RS-485 Output
	Bridge Inputs (E = Excitation Voltage)
D-1511	30 mV In. 5V E/RS-232C Out
D-1512	30 mV In. 5V E/RS-485 Out
D-1521	30 mV In. 10V E/RS-232C Out
D-1522	30 mV In. 10V E/RS-485 Out
D-1531	100 mV In. 5V E/RS-232C Out
D-1532	100 mV In. 5V E/RS-485 Out
D-1541	100 mV In. 10V E/RS-232C Out
D-1542	100 mV In. 10V E/RS-485 Out
	Frequency and Pulse Inputs
D-1601	Frequency Input/RS-232C Output
D-1602	Frequency Input/RS-485 Output
D-1611	Pulse Input/RS-232C Output
D-1621	Event Counter/RS-232C Output
D-1622	Event Counter/RS-485 Output
D-1631	Accumulator Frequency In/RS-232C Out
D-1632	Accumulator Frequency In/RS-485 Out
	Digital Inputs/Outputs
D-1701	7 Digital I/O/RS-232C Output
D-1702	7 Digital I/O/RS-485 Output
D-1711	15 Digital I/O/RS-232C Output
D-1712	15 Digital I/O/RS-485 Output

D-2000 Series: Model	Input/Output
	Voltage Inputs
D-2111	100 mV Input/RS-232C Output
D-2112	100 mV Input/RS-485 Output
D-2121	1V Input/RS-232C Output
D-2122	1V Input/RS-485 Output
D-2131	5V Input/RS-232C Output
D-2132	5V Input/RS-485 Output
D-2141	10V Input/RS-232C Output
D-2142	10V Input/RS-485 Output
	Current Inputs
D-2222	1 mA Input/RS-485 Output
D-2251	4–20 mA Input/RS-232C Output
D-2252	4–20 mA Input/RS-485 Output
	Bridge Inputs (E = Excitation Voltage
D-2511	30 mV In. 5V E/RS-232C Out
D-2512	30 mV In. 5V E/RS-485 Out
D-2521	30 mV In. 10V E/RS-232C Out
D-2522	30 mV In. 10V E/RS-485 Out
D-2531	100 mV In. 5V E/RS-232C Out
D-2532	100 mV In. 5V E/RS-485 Out
D-2541	100 mV In. 10V E/RS-232C Out
	Frequency and Pulse Inputs
D-2601	Frequency Input/RS-232C Output
D-2602	Frequency Input/RS-485 Output
D-2611	Pulse Input/RS-232C Output

D-3000 Series: Model	Output Range/Input
	Voltage Output
D-3121	±1V Output/RS-232C Input
D-3122	±1V Output/RS-485 Input
D-3131	±5V Output/RS-232C Input
D-3141	±10V Output/RS-232C Input
D-3142	±10V Output/RS-485 Input
D-3161	0–1V Output/RS-232C Input
D-3171	0–5V Output/RS-232C Input
D-3172	0–5V Output/RS-485 Input
D-3181	0–10V Output/RS-232C Input
D-3182	0–10V Output/RS-485 Input
	Current Output
D-3251	4–20 mA Out/RS-232C In
D-3252	4–20 mA Out/RS-485 In

D-4000 Series: Model	Output Range/Input
	Voltage Output
D-4121	±1V Output/RS-232C Input
D-4141	±10V Output/RS-232C Input
	Current Output
D-4251	4–20 mA Out/RS-232C In
D-4252	4–20 mA Out/RS-485 In

CONVERTERS/REPEATERS

Features

- ❑ Isolated Bidirectional Data Transmission
- ❑ Allows Networking up to 4,000 Feet
- ❑ Self-Contained Power Supply: +24 Vdc @ 1A
- ❑ 115.2 Kbaud Maximum Communications rate
- ❑ Automatic Supervision of Bus Direction — Transparent to the User

Ordering Guide

Converters/Repeaters

A-1100/115	Converter RS-232 to RS-485 (115 VAC)
A-1100/230	Converter RS-232 to RS-485 (230 VAC)
A-1300/115	Repeater RS-485 (115 VAC)
A-1300/230	Repeater RS-485 (230 VAC)

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